


# BUCKY\_WHL Schematic

2018/04/10

REV : X01

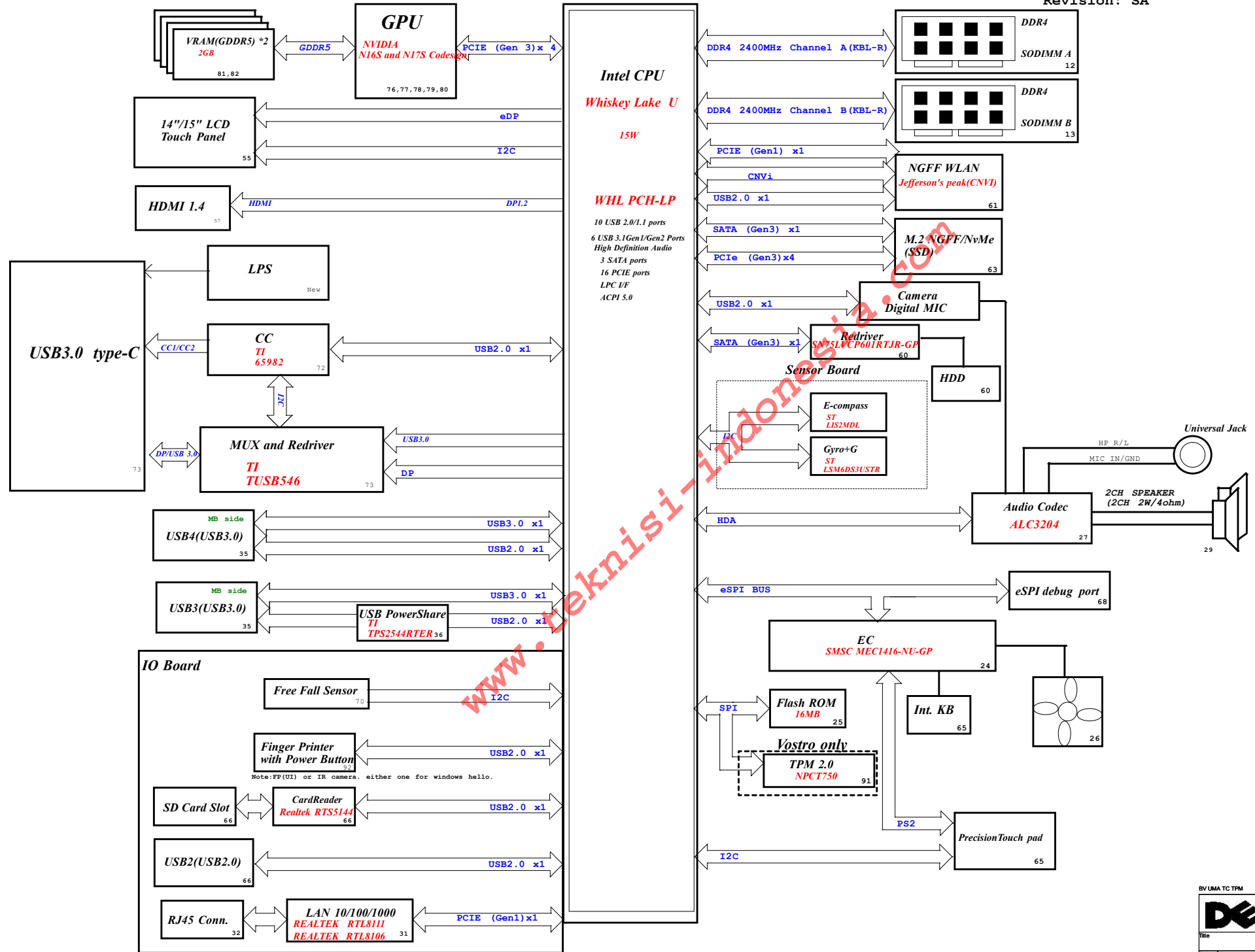
*DY : None Installed*  
*UMA: UMA only installed*  
*OPS: DISCRTE OPTIMUS installed*

BV UMA TC TPM

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Cover Page</b>			
Size A4	Document Number <b>Bucky WHL</b>		Rev <b>SA</b>
Date: Friday, July 13, 2018		Sheet 1	of 105

# Bucky WHL Block Diagram

Project code:  
PCB P/N: 17859  
Revision: SA



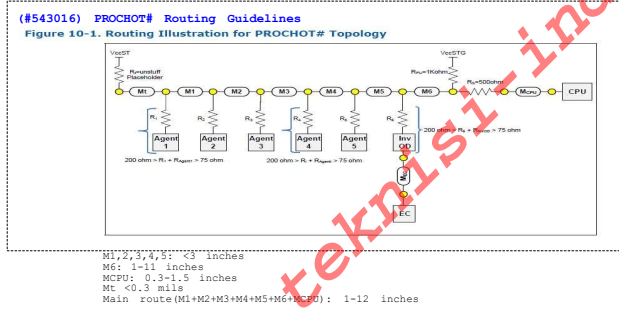
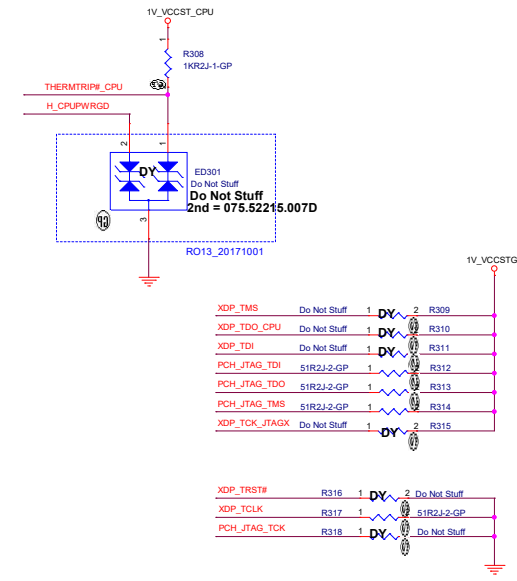
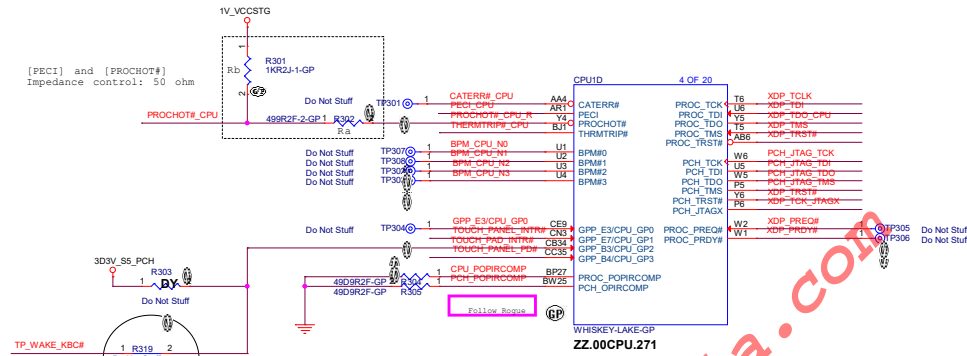
CHARGER	
ISL88739	44
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT
SYSTEM DC/DC	
TPS51225RUKR-GP	45
INPUTS	OUTPUTS
3D3V_PWR 3D3V_S5 5V_PWR 5V_S5	DCBATOUT
CPU Core Power	
NCP81208MNTXG	46~50
NCP81382MNTXG x 2	
NCP81382MNTXG (23e)	
NCP81253MNTBG	
INPUTS	OUTPUTS
VCC_CORE +VCCGT	DCBATOUT
+VCCGT (23e)	DCBATOUT
DDR4 SUS	
RT8231AGQW-GP	51
APL5930KAI-TRG	
INPUTS	OUTPUTS
1D2V_S3 OD5V_S0 2D5V_S3	DCBATOUT
CPU VCCPRIM_CORE 1V	
	11
INPUTS	OUTPUTS
1D0V_S5	+VCCPRIM_CORE
CPU DCDC-V1D00A	
AOZ2262QI-10-GP-U	53
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5
LDO-V1D8V	
APL5930KAI-TRG	54
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5
5V/3V S0	
TPS22966DPUR-GP	40
INPUTS	OUTPUTS
5V_S5 3D3V_S5	5V_S0 3D3V_S0
EOPIO/EDRAM (23e)	
TPS22961DNYT	40
INPUTS	OUTPUTS
1D0V_S5 1D0V_S5	+V_EDRAM_VR +V_EOPIO_VR
3D3V VGA	
AO3419L	86
INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0
VGA CORE	
ISL6271HRTZ-GP-U85	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE
1D5V VGA S0	
Y8288RAC-GP	86
INPUTS	OUTPUTS
DCBATOUT	1D5V_VGA_S0

BV LMA TC TPM

SSID = CPU

24 PECI\_CPU <<<>>>  
24.44.46 PROCHOT#\_CPU <<<>>>  
55 TOUCH\_PANEL\_INTR# <<<>>>  
24.65 TP\_WAKE\_KBC# <<<>>>  
17 H\_CUPWGRD >>>>>>  
55 TOUCH\_PANEL\_PDN# <<<>>>

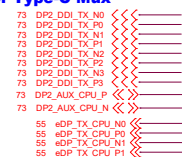
99 XDP\_TCLK <<<>>>  
99 XDP\_TDO\_CPU <<<>>>  
99 XDP\_TDI <<<>>>  
99 XDP\_TMS <<<>>>  
99 XDP\_TCK\_ITAGX >>>>>>  
99 PCH\_ITAG\_TDO >>>>>>  
99 PCH\_ITAG\_TDI >>>>>>  
99 PCH\_ITAG\_TMS >>>>>>



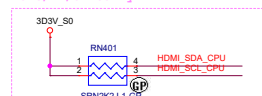
## DP to HDMI2.0



## DP for Type-C Mux



2016/11/01 modify



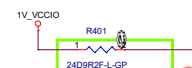
1.65GT Length 6.5" (3VIA)

## DP to HDMI2.0

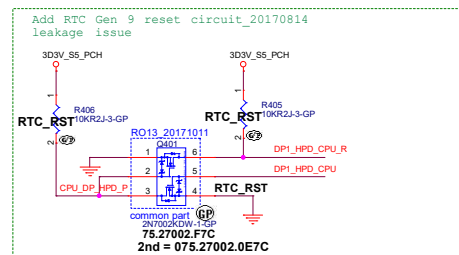
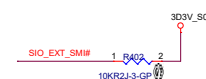
## DP for Type-C Mux

Design Guideline:  
Skylake processor signal eDP\_RCOMP should be connected to the VCCIO rail via a single  $24.9 \pm 1\%$   $\Omega$  resistor

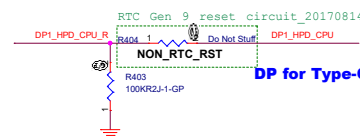
RO13\_20170626



Do Not Stuff TP402



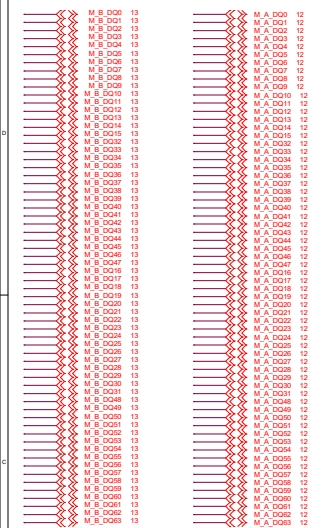
ZZ.00CPU.271



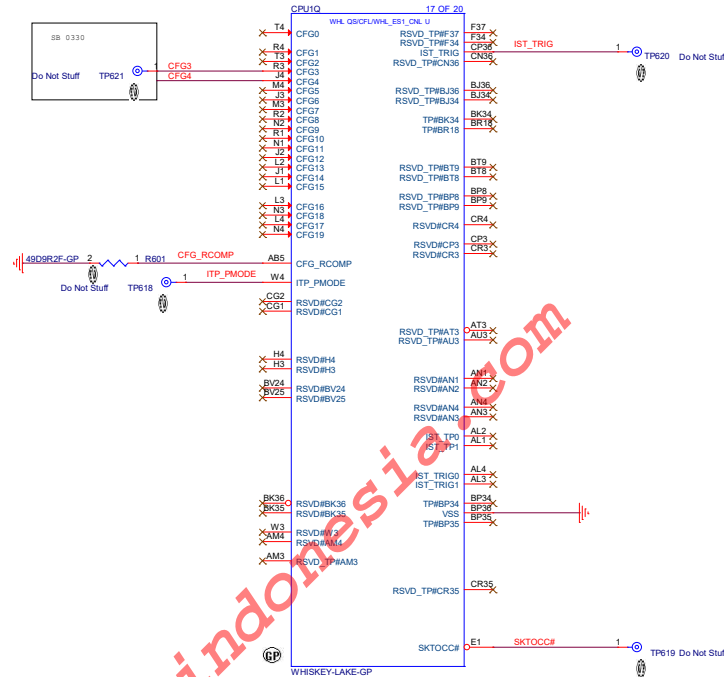
## DP for Type-C Mux

BV UIMA TC TPM





15 CFG3 <<<<  
15 CFG4 <<<<



SKL(#543016) :  
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort\*

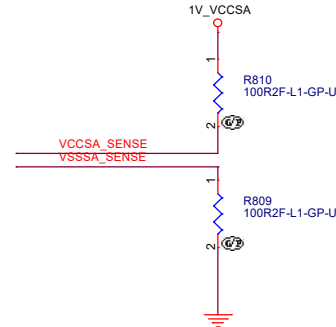
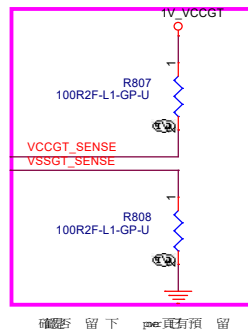
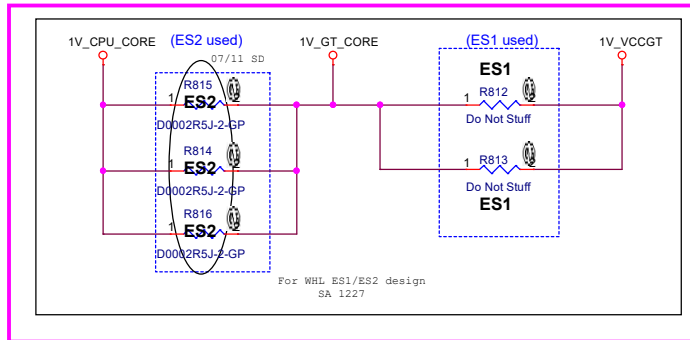
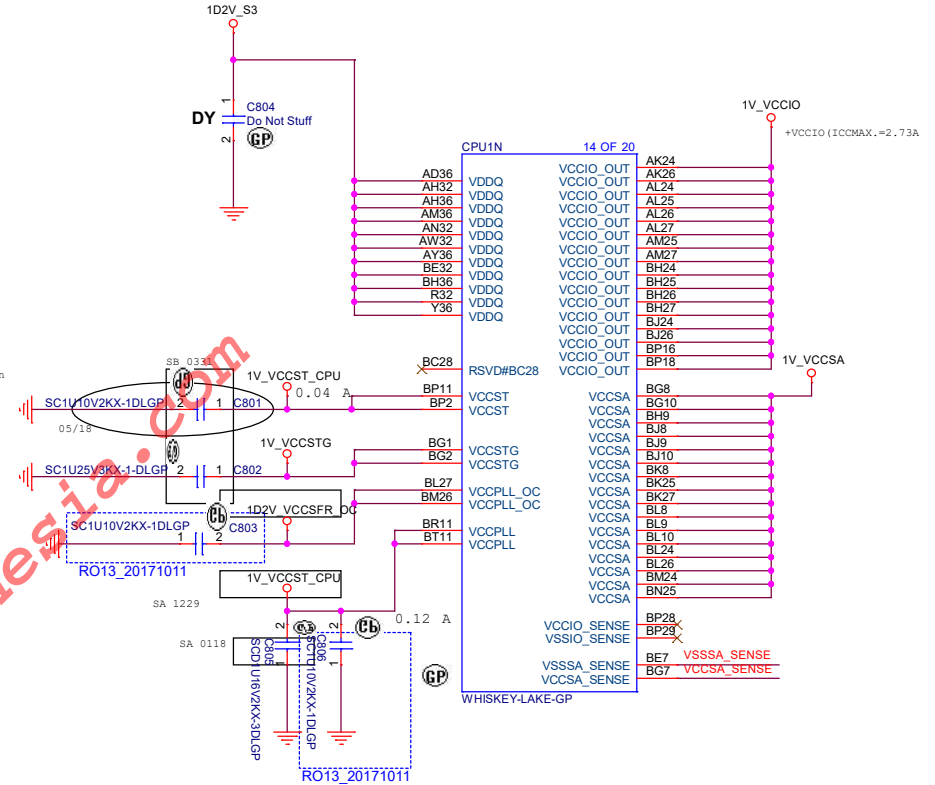
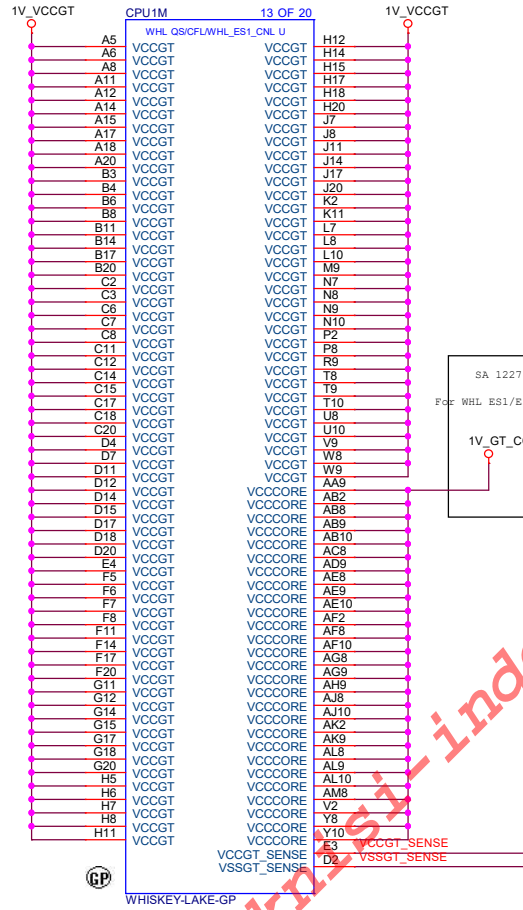
BV LMA TC TPM



46 VSSSA\_SENSE <<<< ———  
46 VCCSA\_SENSE <<<< ———

46 VCCGT\_SENSE <<<< ———  
46 VSSGT\_SENSE <<<< ———

Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE



BV UMA TC TPM

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
Taipei Hsien 221, Taiwan, R.O.C.

Title **CPU (VDDQ/VCC/VCCST/VCCSTG)**

Size A3 Document Number **Bucky WHL** Rev SA

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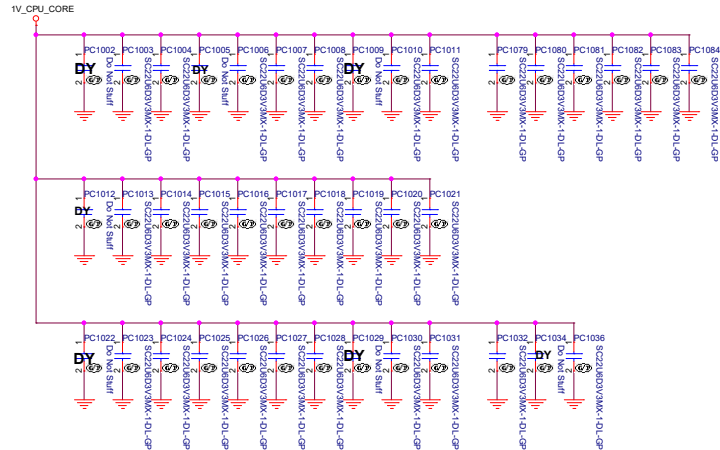
Main Func = CPU

(Blanking)

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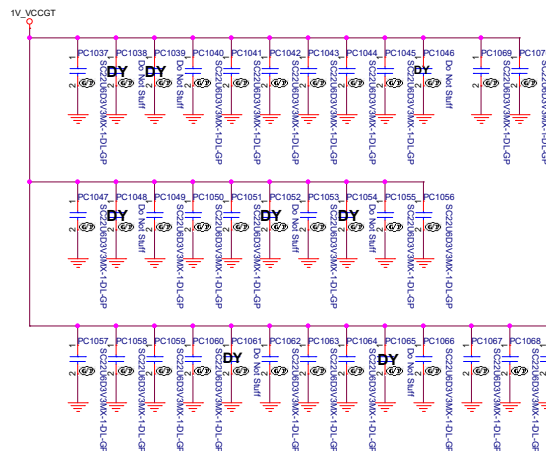
## 1V\_CPU\_CORE

22U 0603 x 39 (3DY)



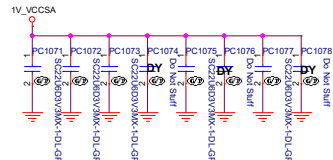
## VCCGT

22U 0603 x 35 (3 DY)



## VCCSA

22U 0603 x 8 (3DY)



## Whiskey Lake U 4+2 Bulk Decoupling Example

Bulk Decoupling Locations	Example	Notes
VCCORE Power Plane at VR output	4x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
VCCGT Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output

**Notes:**  
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.  
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

## Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 1 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCCORE		4x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	Place as close to the package as possible
	8x 10uF 0402		
		18x 47uF 0805 (6.3V)	Place as close to the package as possible. Can be placed on as either Primary or back side cap.

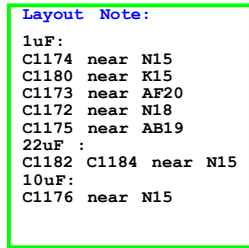
## Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 2 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCCGT	15x 22uF 0603		Place underneath the package
	4x 47uF 0805 (6.3V)		
		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	
VCCSA		4x 0402	Placeholder only.
		7x 10uF 0402	
	6x 10uF 0402		Placeholder Only
	2x 47uF 0805 (6.3V)		
VDDQ		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603		Placeholder Only
	6x 10uF 0402		
VCCIO	4x 1uF 0201		Place underneath the package
		6x 10uF 0402	Place as close to the package as possible
VCCPLL_OC	4x 0402		Placeholder Only
VCCPLL	1x 1uF 0402		Do not merge VCCPLL, VCCPLL_OC and VCCGT to any noisy and high current power rail and do not route them close/adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PLL failing to phase lock.
VCCPLL	1x 0.1uF 0201		Place as close as possible to BGA.
	1x 1uF 0402		Place as close as possible to BGA and can be placed on as either Primary or backside cap.
		1x 0805	Placeholder Only. Can be placed on as either Primary or back side cap.
VCCGT	1x 1uF 0402		
VCCSTS	1x 1uF 0402		

**Notes:**  
1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ~ 250kHz e.g., 1MHz switching VR  
2. Component placement order: Package edge > 0402 caps > 0603 caps > 0805 caps > Bulk caps > Power source.

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PCH DERIVED RAILS UNSLICED GT VCCIO



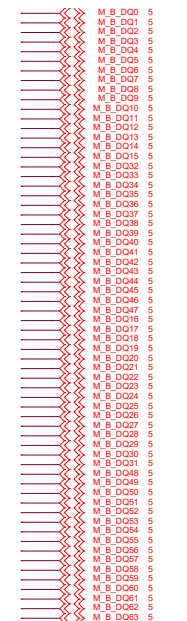
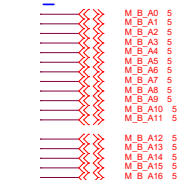
Title			
CPU_(Power CAP2)			
Size A3	Document	Number	Rev
		Bucky WHL	SA
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## DDR DATA



5 M\_B\_DQS\_DN[7:0] << >>

5 M\_B\_DQS\_DP[7:0] << >>

## DDR CMD/ADD

```

5 M B ACT N >>>_____
5 M B ALERT N >>>_____
5 M B PARITY >>>_____

```

5 V\_SM\_VREF\_CNTB &gt;&gt;&gt;\_\_\_\_\_

## DDR CTRL

5 M\_B\_CS#0 >>> \_\_\_\_\_  
5 M\_B\_CS#1 >>> \_\_\_\_\_

5 M\_B\_CKE0 >>> \_\_\_\_\_  
5 M\_B\_CKE1 >>> \_\_\_\_\_

DDR CLOCK

```

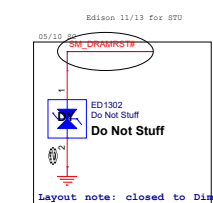
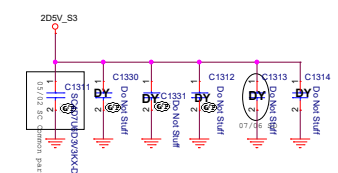
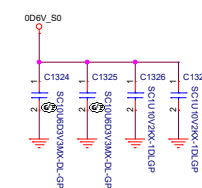
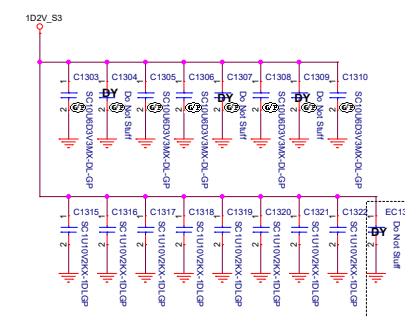
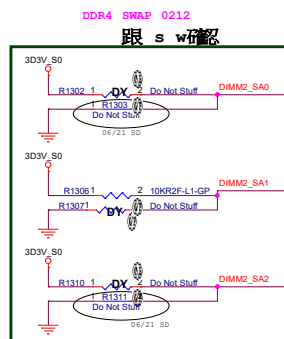
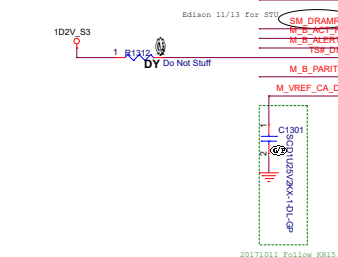
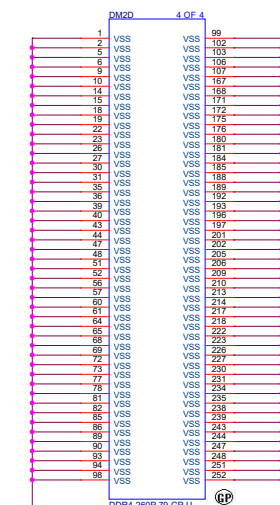
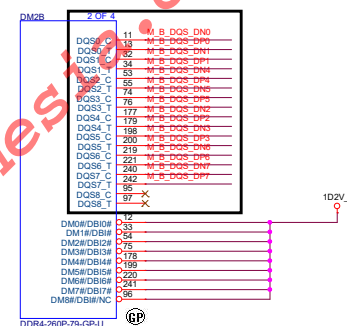
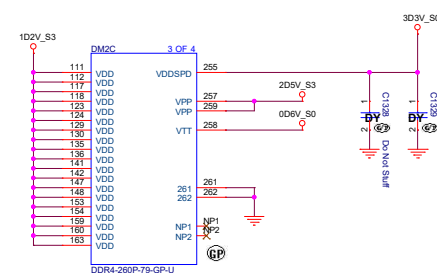
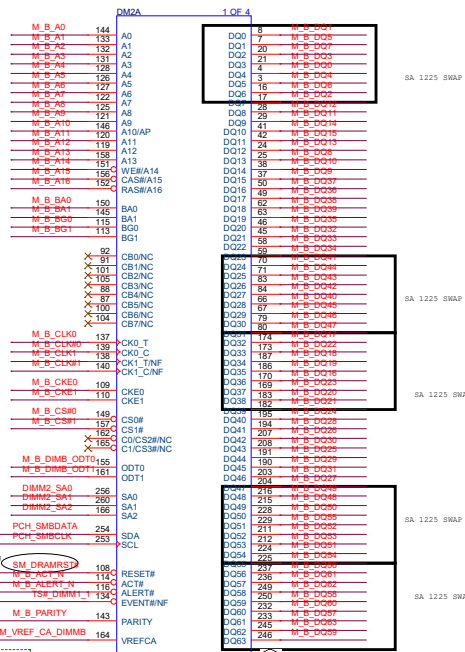
5 M_B_CLK0 >>> _____
5 M_B_CLK#0 >>> _____

5 M_B_CLK1 >>> _____
5 M_B_CLK#1 >>> _____

```

## DDR OTHERS

5,12,13 SM\_DRAMRST# >>>—  
12,18,65 PCH\_SMBDATA <<<<<<—  
12,18,65 PCH\_SMBCLK <<<<<<—  
5,12,13 SM\_DRAMRST# >>>—



Layout note: closed to Dinner

(Blanking)

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**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title **DDR (RSVD) (DDR4-CHA1)**

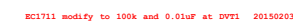
Size A4	Document Number <b>Bucky WHL</b>	Rev <b>SA</b>
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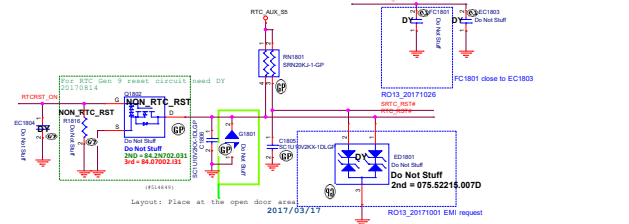
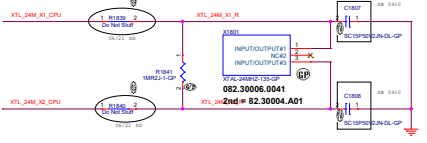
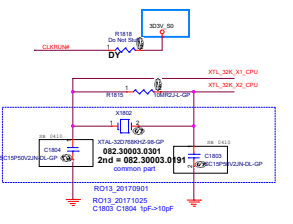
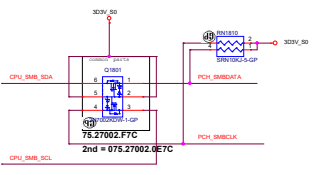
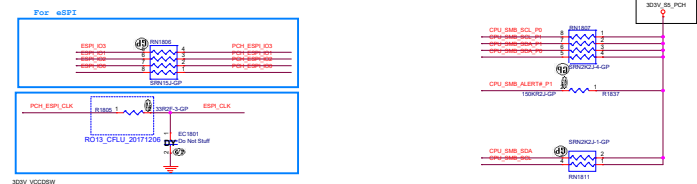
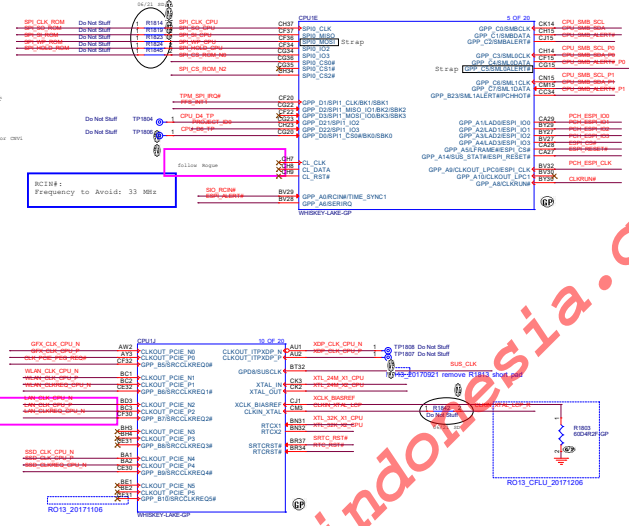
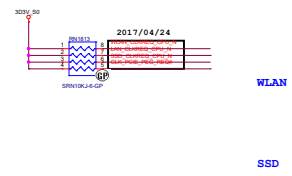
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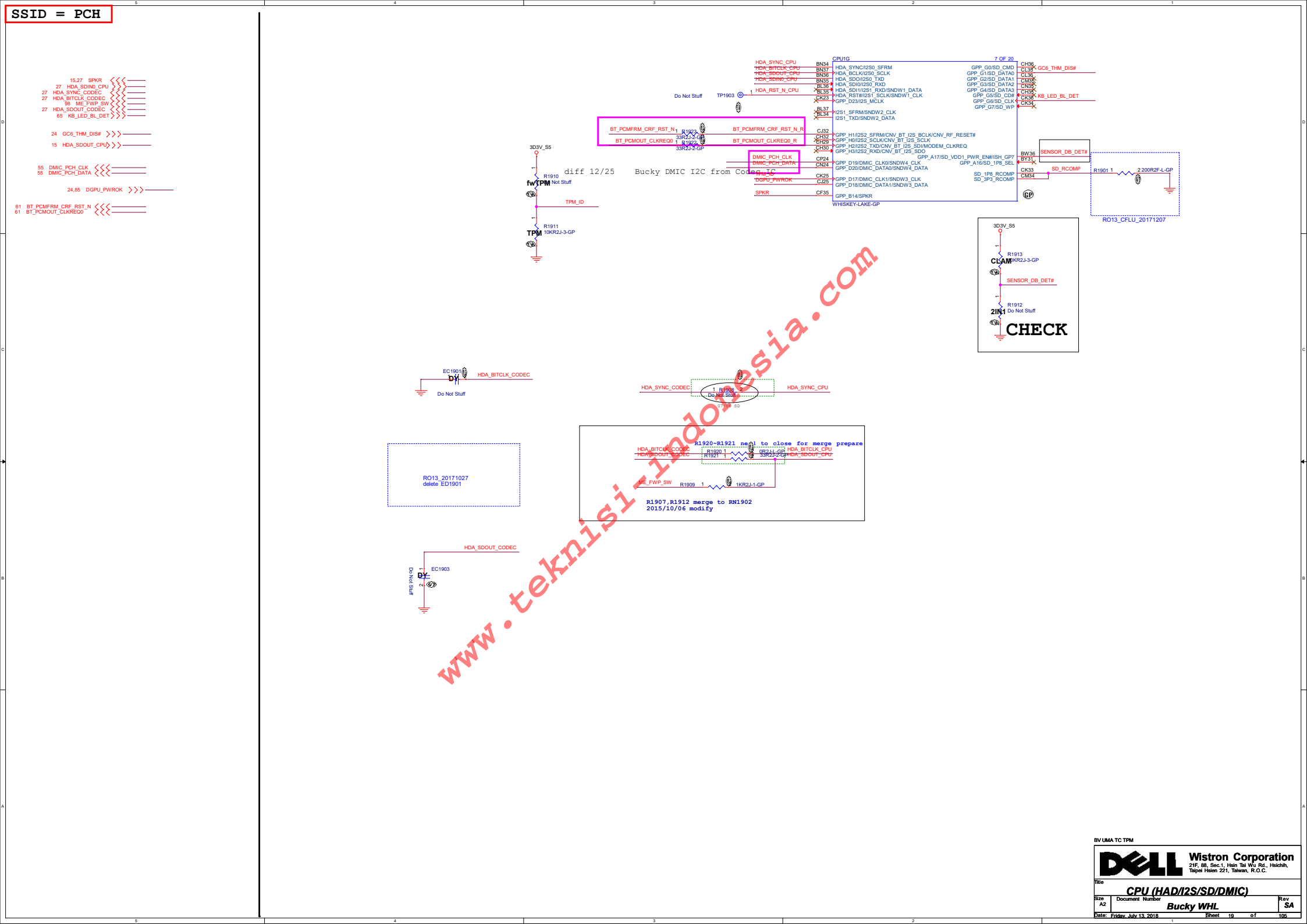
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**PCH strap pin:**





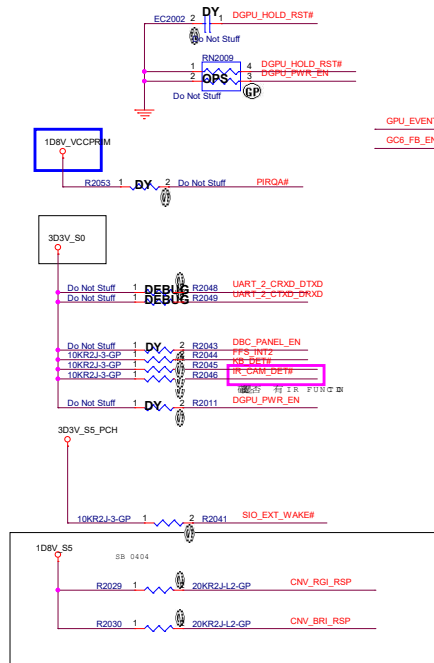
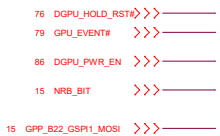
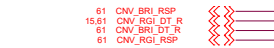
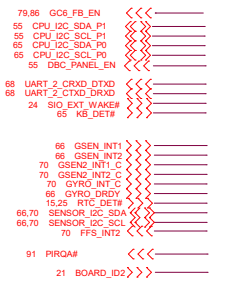




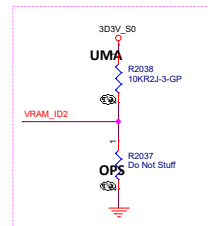
BV LMA TC TPM



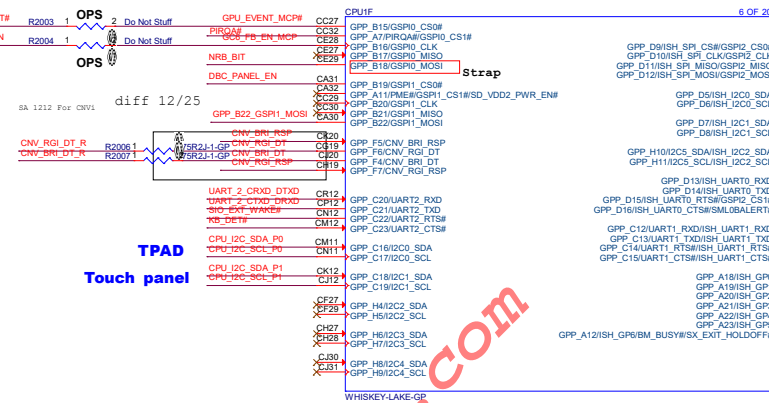
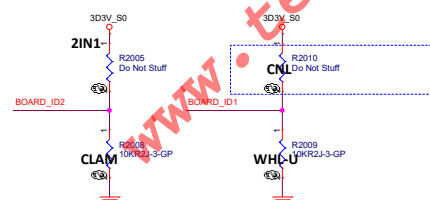
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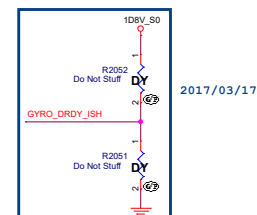
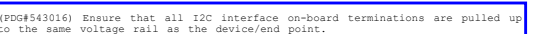
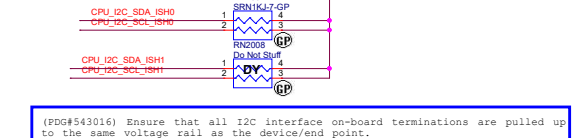
2016/11/07 modify



	H(10K)	L(10K)
VRAM_ID2	UMA	OPS
BOARD_ID2	2IN1	CLAM
BOARD_ID1	CNL	WHL-U
NB_MODE#	2IN1	CLAM

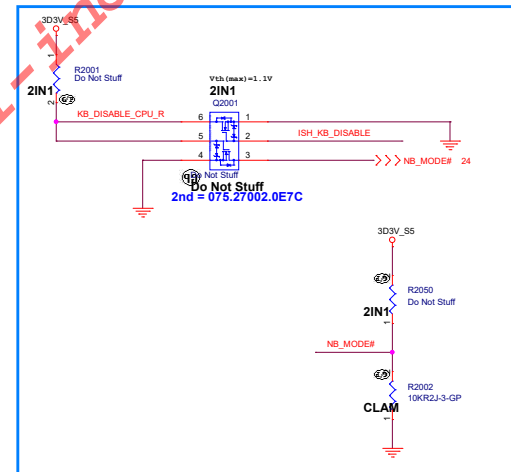


**TPAD**  
**Touch panel**



2017/03/17

(PDG#543016) If the UART/GPIO functionality is also not used, the signals can be left as no-connect.





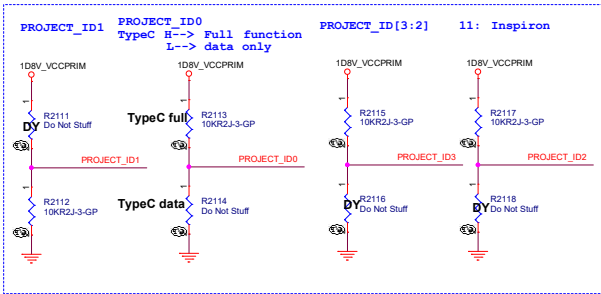
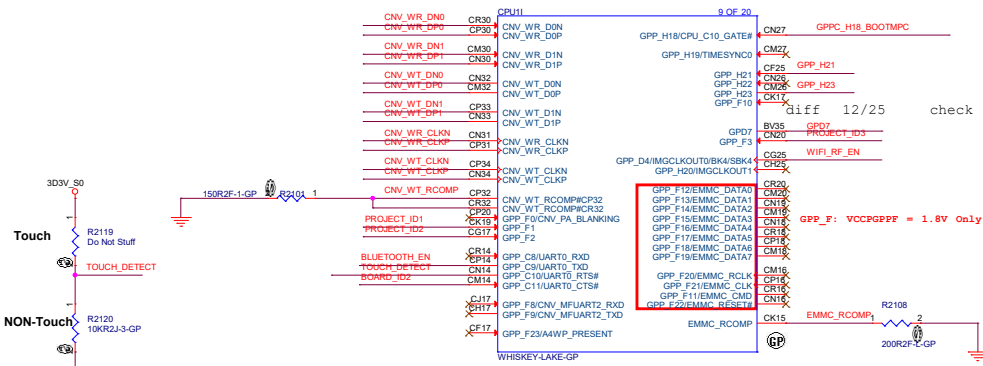
SSID = PCH

SSID = PCH

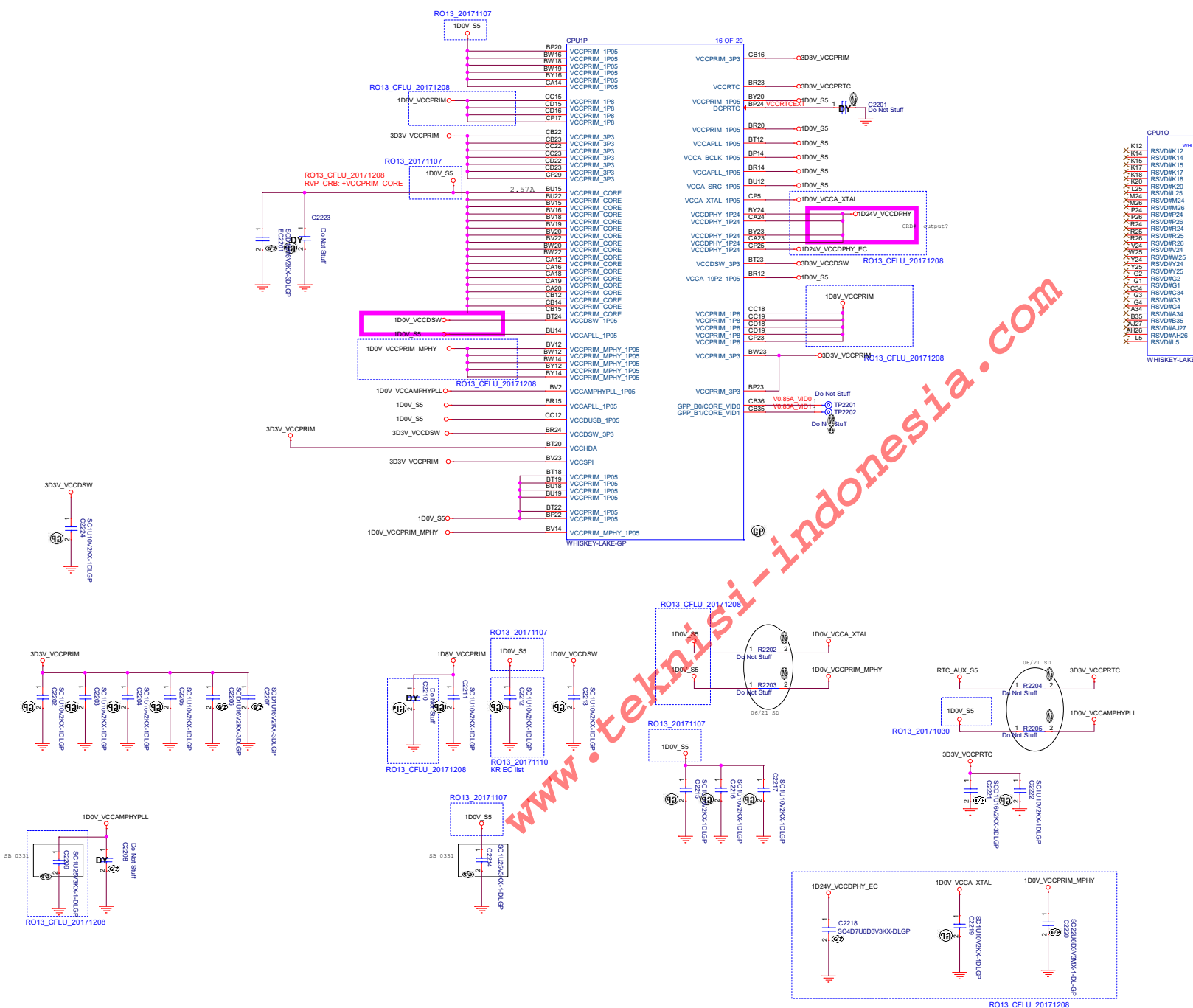
40 GPPC\_H18\_BOOTMPC <<<—  
61 WIFI\_RF\_EN <<<—  
61 BLUETOOTH\_EN <<<—  
20 BOARD\_ID2 <<<—  
15 GPP\_H23 >>>—  
15 GPP\_H21 <<<—

61 CNV\_WT\_CLKN >>>—  
61 CNV\_WT\_CLKP >>>—  
61 CNV\_WT\_DP0 >>>—  
61 CNV\_WT\_DP1 >>>—  
61 CNV\_WT\_DN1 >>>—  
61 CNV\_WR\_CLKN >>>—  
61 CNV\_WR\_CLKP >>>—  
61 CNV\_WR\_DP0 >>>—  
61 CNV\_WR\_DP1 >>>—  
61 CNV\_WR\_DN1 >>>—

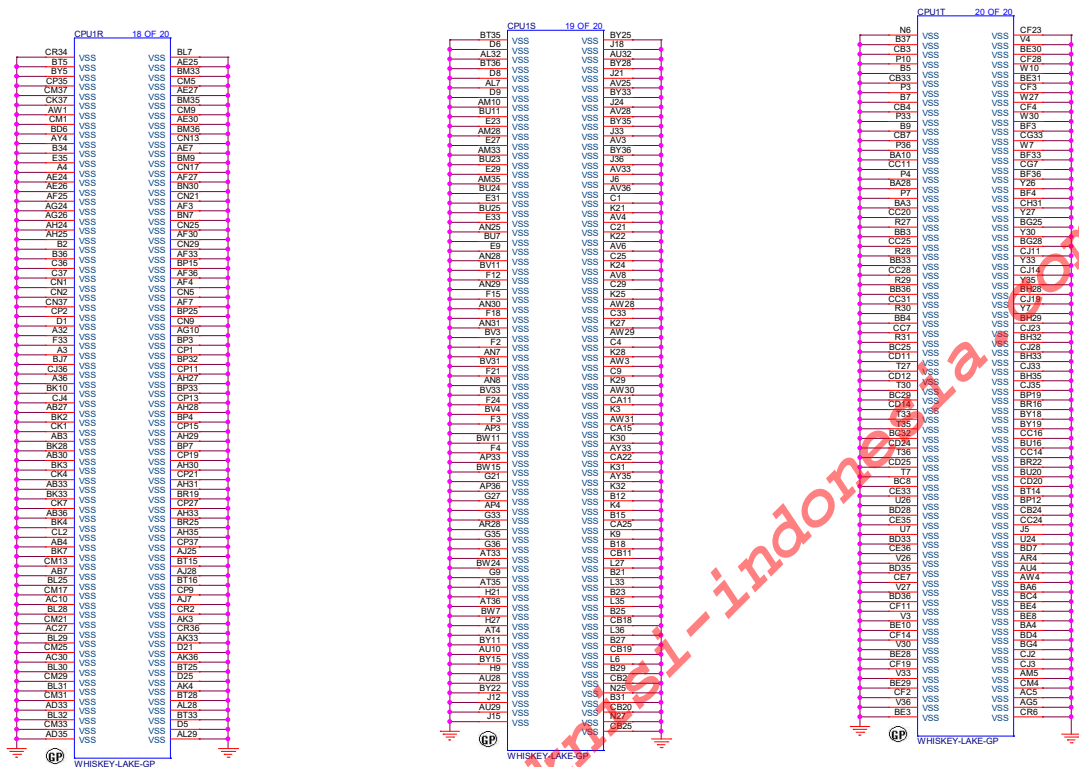
18 PROJECT\_ID0 <<<—  
15 GPD7 <<<—



	Hi(10K)	Lo(10K)	Note
PROJECT_ID0	TypeC full	TypeC data	TypeC function det
PROJECT_ID1	Non	Non	follow Rogue define
PROJECT_ID2	Non	Non	
PROJECT_ID3	Non	Non	



Layout Note:							
Decoupling and Power Connection Requirements for WHL U PCH (Sheet 1 of 2)							
Voltage Supply	Area	PCH Pins sharing power	Value	Size	Quantity	Placement type (Runway / Edge)	Place capacitor(s) near ball(s)
V1.65A	VCCA_1P92_1P03	BR12	-	-	-	-	-
	VCCA_OC_1P03	BF14	-	-	-	-	-
	VCCA_SBC_1P03	BU12	-	-	-	-	-
	VCCA_XTAL_1P03	CP9	1uF	0402	1	E	CP9
	VCCDUSB_1P03	CC12	-	-	-	-	-
	VCCPRIM_1P03	BR12, BR14, BR15, BR16, BP20, BW12, BW19, BW20, BW21, BW22, CA18, CA19, CA20, CB12, CB14, CB15	1uF	0402	1	E	BP20
	VCCMPHYT0N_1P03	BV12, BV19, BV20, BV21, BV12, BV14, BV16, BV18, BV19	22uF	0603	1	E	BV12
	VCCAMPHYRL_1P03	BV2	1uF	0402	1	E	BV2
	VCCPRIM_CORE	BU12, BU22, BV15, BV19, BV20, BV22, BW20, BW21, BW22, CA18, CA19, CA20, CB12, CB14, CB15	1uF	0402	1	E	BV19, Note 1
	V1.9A / V0.58A	CC18, CC19, CC18, CC19, CP23, CC19, CC18, CC19, CP17	1uF	0402	1	E	CP17, Note 1
V1.8A	VCCPRIM_1P8	CC18, CC19, CC18, CC19, CP23, CC19, CC18, CC19, CP17	1uF	0402	1	E	CP17, Note 1
Voltage Supply	Area	PCH Pins sharing power	Value	Size	Quantity	Placement type (Runway / Edge)	Place capacitor(s) near ball(s)
V3.3A	VCCPRIM_3P3	CB22, CB23, CB24, CB25, CB26, CB27, CB28, CB29, CB30, CB31, CB32, CB33, CB34, CB35, CB36, CB37, CB38, CB39, CB40, CB41, CB42, CB43, CB44, CB45, CB46, CB47, CB48, CB49, CB50, CB51, CB52, CB53, CB54, CB55, CB56, CB57, CB58, CB59, CB60, CB61, CB62, CB63, CB64, CB65, CB66, CB67, CB68, CB69, CB70, CB71, CB72, CB73, CB74, CB75, CB76, CB77, CB78, CB79, CB80, CB81, CB82, CB83, CB84, CB85, CB86, CB87, CB88, CB89, CB90, CB91, CB92, CB93, CB94, CB95, CB96, CB97, CB98, CB99, CB100, CB101, CB102, CB103, CB104, CB105, CB106, CB107, CB108, CB109, CB110, CB111, CB112, CB113, CB114, CB115, CB116, CB117, CB118, CB119, CB120, CB121, CB122, CB123, CB124, CB125, CB126, CB127, CB128, CB129, CB130, CB131, CB132, CB133, CB134, CB135, CB136, CB137, CB138, CB139, CB140, CB141, CB142, CB143, CB144, CB145, CB146, CB147, CB148, CB149, CB150, CB151, CB152, CB153, CB154, CB155, CB156, CB157, CB158, CB159, CB160, CB161, CB162, CB163, CB164, CB165, CB166, CB167, CB168, CB169, CB170, CB171, CB172, CB173, CB174, CB175, CB176, CB177, CB178, CB179, CB180, CB181, CB182, CB183, CB184, CB185, CB186, CB187, CB188, CB189, CB190, CB191, CB192, CB193, CB194, CB195, CB196, CB197, CB198, CB199, CB200, CB201, CB202, CB203, CB204, CB205, CB206, CB207, CB208, CB209, CB210, CB211, CB212, CB213, CB214, CB215, CB216, CB217, CB218, CB219, CB220, CB221, CB222, CB223, CB224, CB225, CB226, CB227, CB228, CB229, CB230, CB231, CB232, CB233, CB234, CB235, CB236, CB237, CB238, CB239, CB240, CB241, CB242, CB243, CB244, CB245, CB246, CB247, CB248, CB249, CB250, CB251, CB252, CB253, CB254, CB255, CB256, CB257, CB258, CB259, CB260, CB261, CB262, CB263, CB264, CB265, CB266, CB267, CB268, CB269, CB270, CB271, CB272, CB273, CB274, CB275, CB276, CB277, CB278, CB279, CB280, CB281, CB282, CB283, CB284, CB285, CB286, CB287, CB288, CB289, CB290, CB291, CB292, CB293, CB294, CB295, CB296, CB297, CB298, CB299, CB300, CB301, CB302, CB303, CB304, CB305, CB306, CB307, CB308, CB309, CB310, CB311, CB312, CB313, CB314, CB315, CB316, CB317, CB318, CB319, CB320, CB321, CB322, CB323, CB324, CB325, CB326, CB327, CB328, CB329, CB330, CB331, CB332, CB333, CB334, CB335, CB336, CB337, CB338, CB339, CB340, CB341, CB342, CB343, CB344, CB345, CB346, CB347, CB348, CB349, CB350, CB351, CB352, CB353, CB354, CB355, CB356, CB357, CB358, CB359, CB360, CB361, CB362, CB363, CB364, CB365, CB366, CB367, CB368, CB369, CB370, CB371, CB372, CB373, CB374, CB375, CB376, CB377, CB378, CB379, CB380, CB381, CB382, CB383, CB384, CB385, CB386, CB387, CB388, CB389, CB390, CB391, CB392, CB393, CB394, CB395, CB396, CB397, CB398, CB399, CB400, CB401, CB402, CB403, CB404, CB405, CB406, CB407, CB408, CB409, CB410, CB411, CB412, CB413, CB414, CB415, CB416, CB417, CB418, CB419, CB420, CB421, CB422, CB423, CB424, CB425, CB426, CB427, CB428, CB429, CB430, CB431, CB432, CB433, CB434, CB435, CB436, CB437, CB438, CB439, CB440, CB441, CB442, CB443, CB444, CB445, CB446, CB447, CB448, CB449, CB450, CB451, CB452, CB453, CB454, CB455, CB456, CB457, CB458, CB459, CB460, CB461, CB462, CB463, CB464, CB465, CB466, CB467, CB468, CB469, CB470, CB471, CB472, CB473, CB474, CB475, CB476, CB477, CB478, CB479, CB480, CB481, CB482, CB483, CB484, CB485, CB486, CB487, CB488, CB489, CB490, CB491, CB492, CB493, CB494, CB495, CB496, CB497, CB498, CB499, CB500, CB501, CB502, CB503, CB504, CB505, CB506, CB507, CB508, CB509, CB510, CB511, CB512, CB513, CB514, CB515, CB516, CB517, CB518, CB519, CB520, CB521, CB522, CB523, CB524, CB525, CB526, CB527, CB528, CB529, CB530, CB531, CB532, CB533, CB534, CB535, CB536, CB537, CB538, CB539, CB540, CB541, CB542, CB543, CB544, CB545, CB546, CB547, CB548, CB549, CB550, CB551, CB552, CB553, CB554, CB555, CB556, CB557, CB558, CB559, CB560, CB561, CB562, CB563, CB564, CB565, CB566, CB567, CB568, CB569, CB570, CB571, CB572, CB573, CB574, CB575, CB576, CB577, CB578, CB579, CB580, CB581, CB582, CB583, CB584, CB585, CB586					

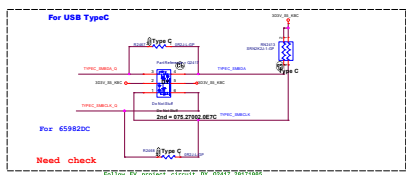


Skylake U Processor Corner NCTF Motherboard Test Point Example

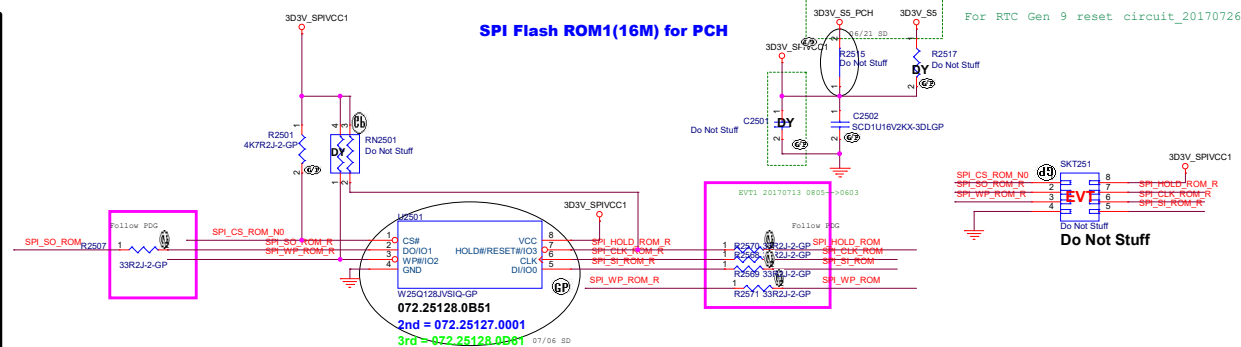
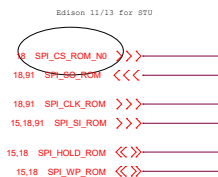
Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	
A5	NCTFVSS	Test Point (TP)	Corner A1
A70	NCTFVSS	Test Point (TP)	
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

SV LMA TC TPM

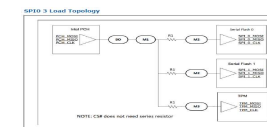
**DELL** Wistron Corporation  
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## Main Func = SPI Flash

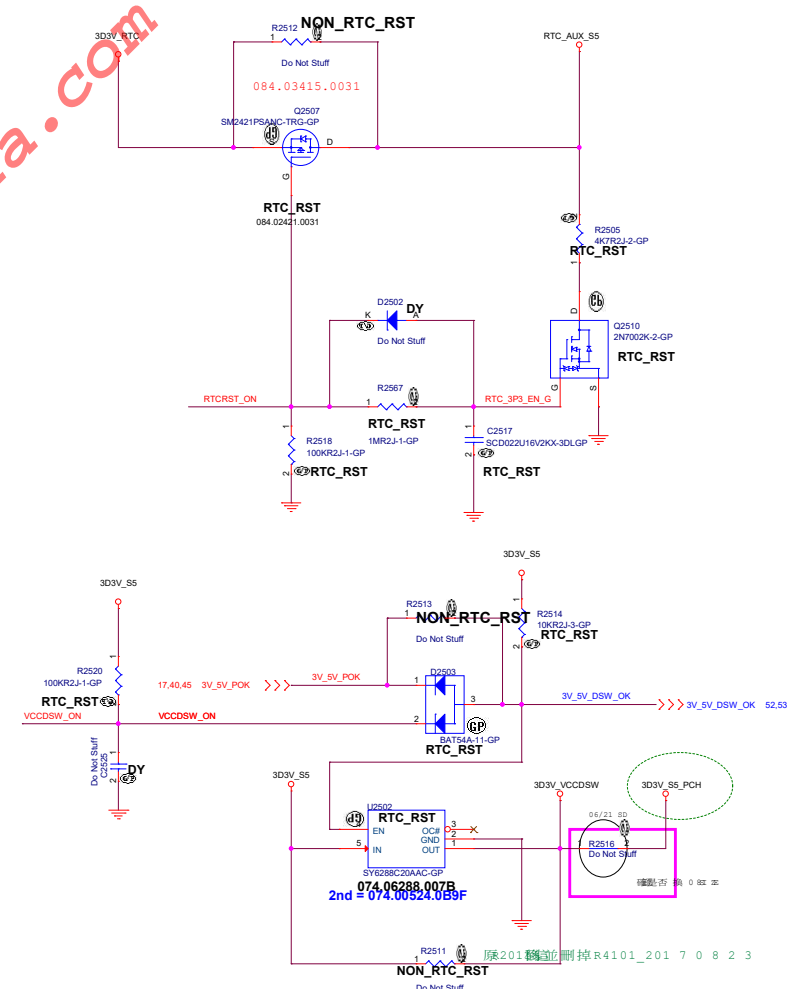
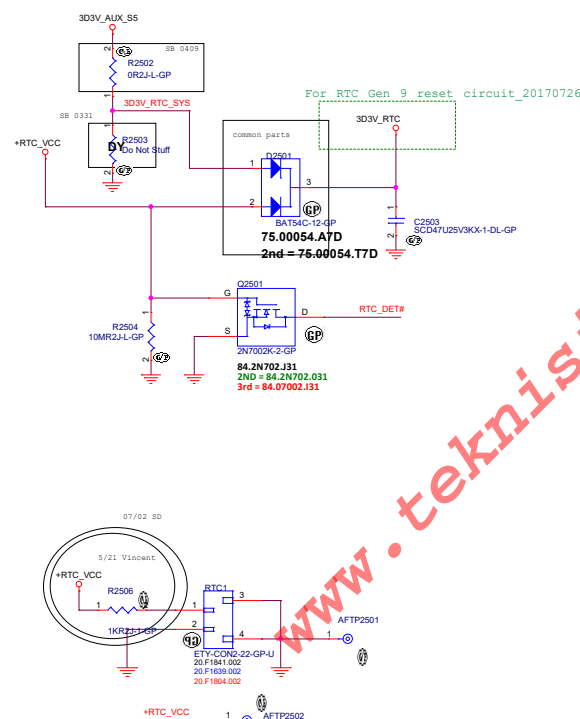


The CFL PCH supports TPM through SPI0 bus. The topology below was a full configuration which consist of 2 SPI0 Flash and 1 TPM device. The system can be configured with 1 SPI0 Flash and 1 TPM device.



Segment	Time Type	Reference	Via Count	Max Length, mm		Max Length, mils	
				Segment	Total	Segment	Total
Notes:							
1.							
2.							
3.							
4.							
5.							

**Main Func = RTC**



Add RTC Gen 9 reset circuit 20170726

RV LIMA TC TP



Title			
<b>Flash</b>			
Size A2	Document Number		Rev
	<b>Bucky WHL</b>		<b>SA</b>
Date:	Friday, July 13, 2018	Sheet 25 of	105

Layout Note:  
Signal Routing Guideline:  
Trace width = 15mil

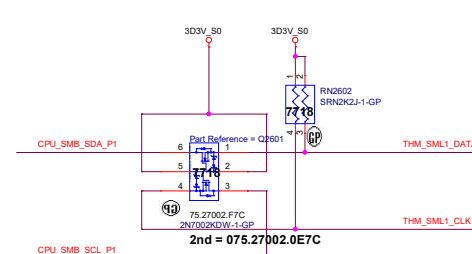
18,24,79 CPU\_SMB\_SDA\_P1 <<>  
18,24,79 CPU\_SMB\_SCL\_P1 <<>

17,24,40 RESET\_OUT# >>>  
40 PURE\_HW\_SHUTDOWN# <<<

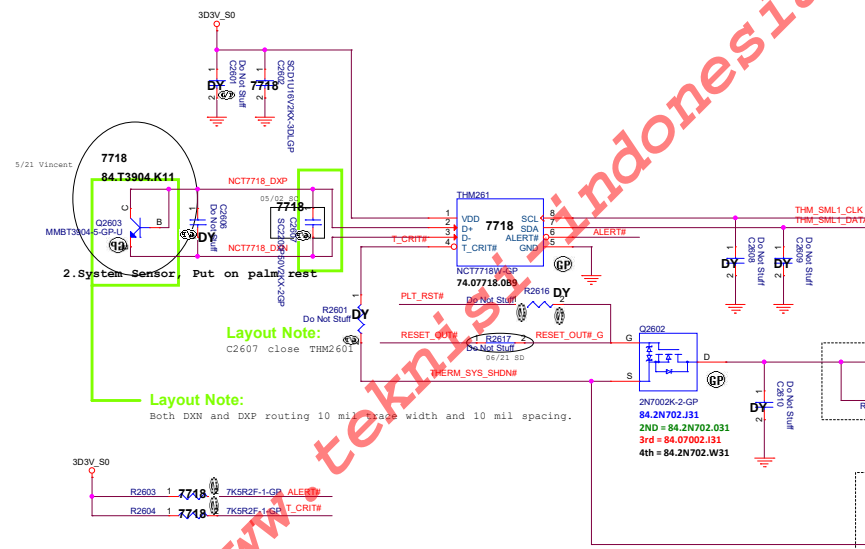
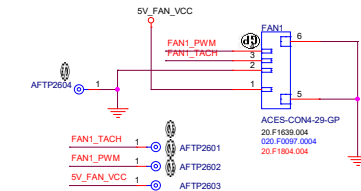
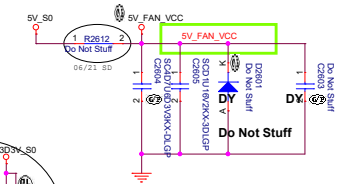
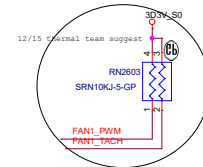
24 CMP\_VOUT0 >>>  
24 CMP\_VIND\_R <<<

24 FAN1\_PWM >>>  
24 FAN1\_TACH <<<

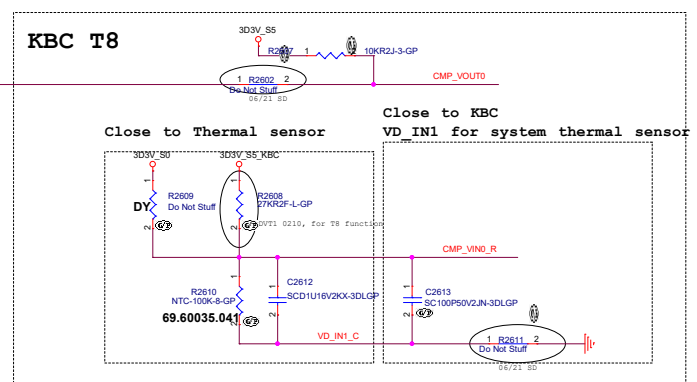
17,61,63,66,76,91 PLT\_RST# >>>



PWM/TACH level 25V



TEMPERATURE (°C)	T_CRIT#					
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ	
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



BV LMA TC TPM

Main Func = Audio

```

19  HDA_SDIN0_CPU      <<<-----
19  HDA_SDOUT_CODEC    >>>-----
19  HDA_SYNC_CODEC     >>>-----
19  HDA_BITCLK_CODEC   >>>-----

```

```

29 AUD_SPK_R+ <<< _____
29 AUD_SPK_R- <<< _____
29 AUD_SPK_L+ <<< _____
29 AUD_SPK_L- <<< _____

```

```

55 DMIC_SDA_CODEC<<<-----
55 DMIC_SCL_CODEC  <<<-----
17,40,68 PM SLP S3#>>>-----

```

```

24 NB_Mute# >>>_____
15,19 SPKR   >>>_____
24 BEEP      >>>_____
29 AUD_SENSE >>>_____

```

```

29  LINE1_VREFO  <<< _____
29  MIC2_VREFO  <<< _____
29  AUD_HP1_JACK_L <<< _____
29  AUD_HP1_JACK_R <<< _____
29  LINE1_L     >>> _____
29  LINE1_R     >>> _____

```

29 LINE1\_L >>>\_\_\_\_\_

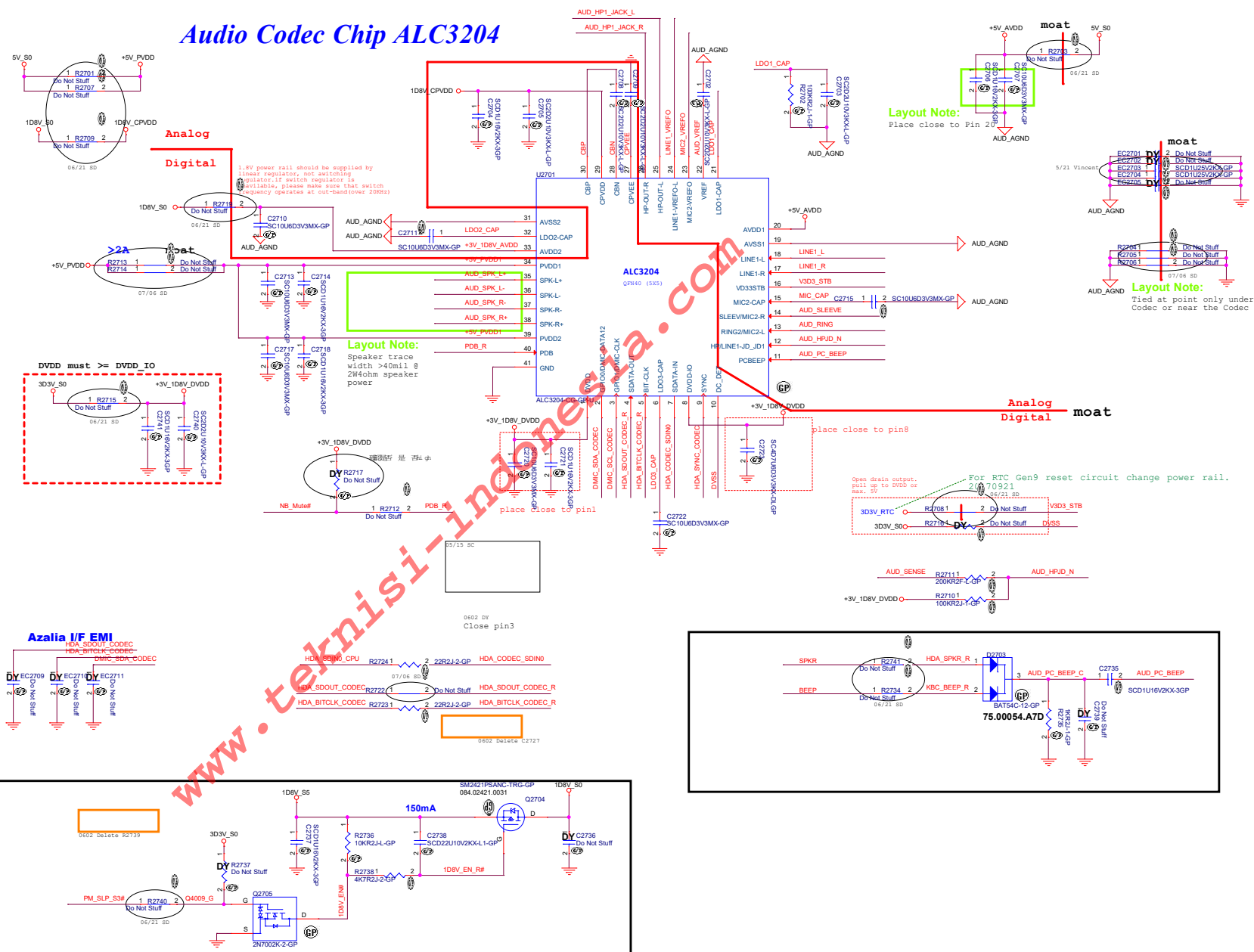
29 LINE1\_R >>>\_\_\_\_\_

29 AUD\_SLEEVE <<< \_\_\_\_\_

29 AUD\_RING <<< \_\_\_\_\_

29. AUD RING &lt;&lt;&lt;\_\_\_\_\_

## Audio Codec Chip ALC3204



(Blanking)

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Size  
A4

Document Number

**Bucky WHL**

Rev  
**SA**

Date: Friday, July 13, 2018

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Title <b>(Reserved)</b>			
Size A4	Document Number <b>Bucky WHL</b>		Rev <b>SA</b>
Date: Friday, July 13, 2018		Sheet 30 of	105

Main Func = LAN

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Title

LAN RTL8106

Size

Document Number

Rev

Custom

Bucky WHL

SA

Date: Friday, July 13, 2018

1

Sheet

31


of

105

Main Func = LAN

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Title

XFOM&RJ45

SA

Size  
A3

Document Number  
Bucky WHL

Date: Friday, July 13, 2018


Rev  
SA

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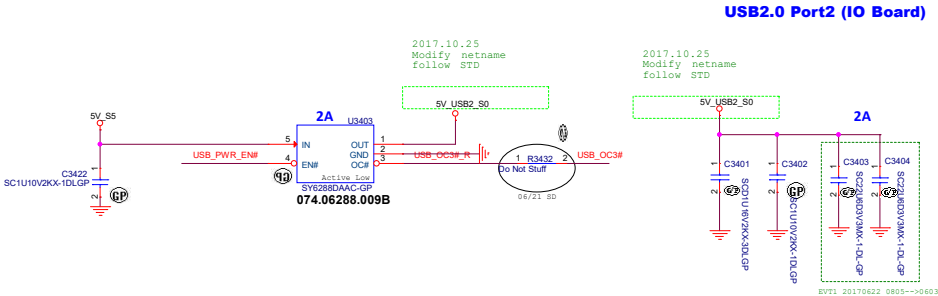
Main Func = Card Reader

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Title			
<b>Card Reader-RTS5170</b>			
Size A4	Document Number		Rev <b>SA</b>
Date: Friday, July 13, 2018		Sheet 33 of	105

Main Func = USB2.0



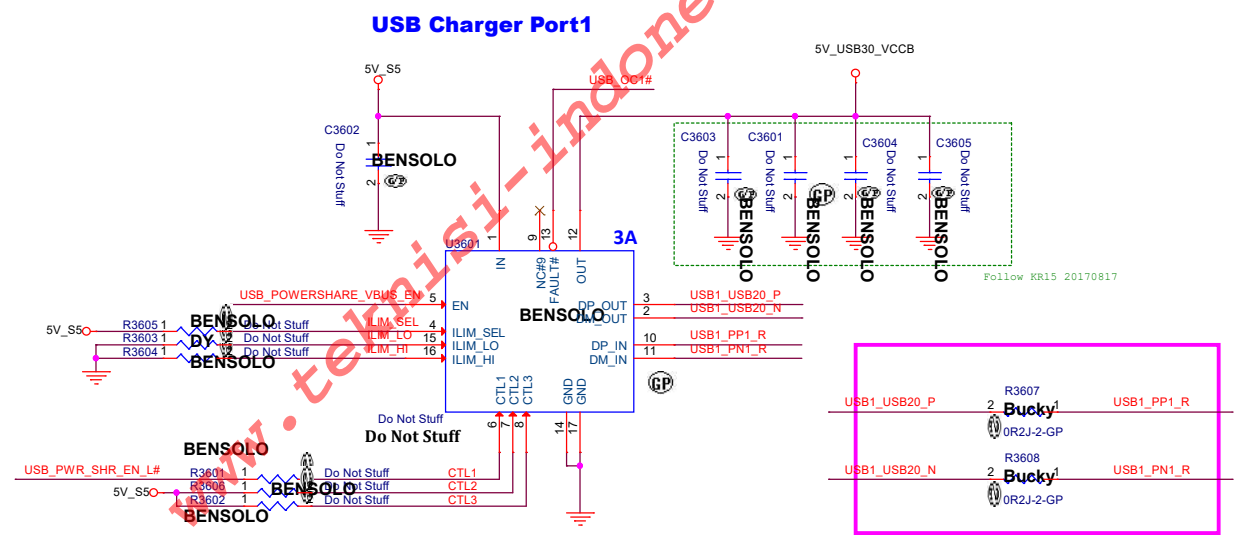
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SV LMA TC TPM



Main Func = USB Charger

- 24,34,35 USB\_PWR\_EN# >>>
- 24 USB\_POWERSHARE\_VBUS\_EN >>>
- 24 USB\_PWR\_SHR\_EN\_L# >>>
- 16 USB\_OC1# <<<
- 35 USB1\_PN1\_R <<>
- 35 USB1\_PP1\_R <<>
- 16 USB1\_USB20\_N <<>
- 16 USB1\_USB20\_P <<>



Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

BV UMA TC TPM

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Title

USB Charger

Size A3

Document Number

Bucky WHL

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Rev SA



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Title			
<b>USB3.0 PORT</b>			
Size	Document	Number	Rev
A4		<b>Bucky WHL</b>	<b>SA</b>
Date: Friday, July 13, 2018		Sheet 37 of	105

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Title			
<b>Reserved</b>			
Size	Document Number		Rev
A4	<b>Bucky WHL</b>		<b>SA</b>
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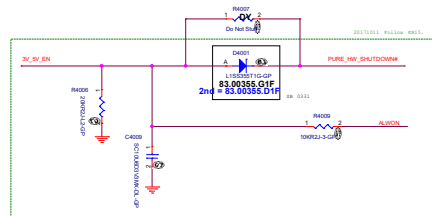
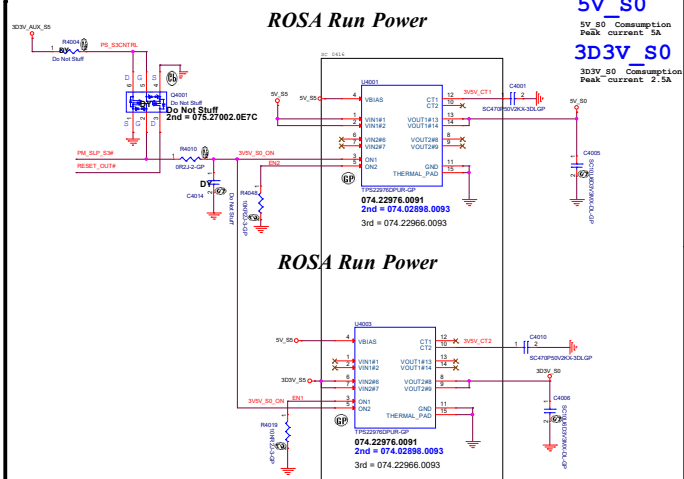
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BV LMA TC TPM

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Title			
(RSVD)			
Size	Document	Number	Rev
A2	Bucky WHL		SA
Date: Friday, July 13, 2018			
Sheet		39	of 106

### *ROSA Run Power*

5V\_S0  
5V S0 Consumption  
Peak current 5A  
3D3V\_S0

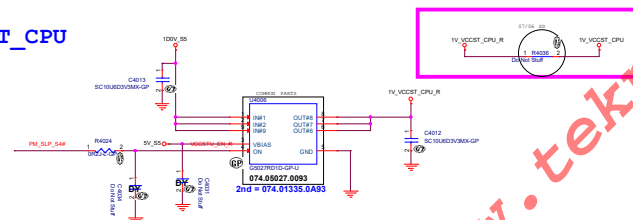


## MANAGEMENT RAIL POWER GENERATION

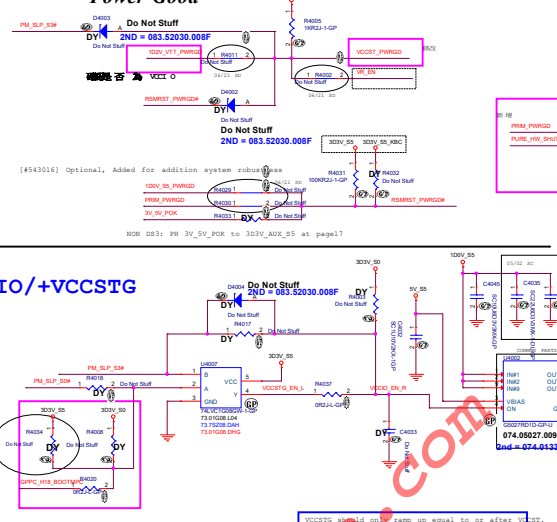
VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

VCCST CPU

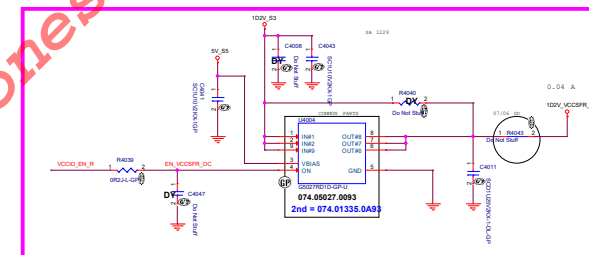
VCCST CPU



## +VCCIO/+VCCSTG



## 1D2V VCCSFR OC




+V1.8S0

Main Func = Power & Sequence

原410機一用R2516\_2017 0 82 3

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BV UMA TC TPM

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Title <b>Connected_Standby(1/2)+DS3</b>		
Size A4	Document Number <b>Bucky WHL</b>	Rev <b>SA</b>
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Title **Connected\_Standby(2/2)**

Size A4	Document Number <b>Bucky WHL</b>	Rev <b>SA</b>
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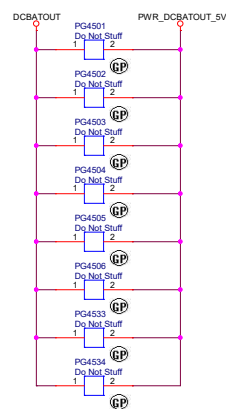
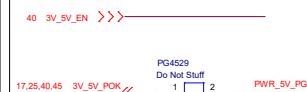
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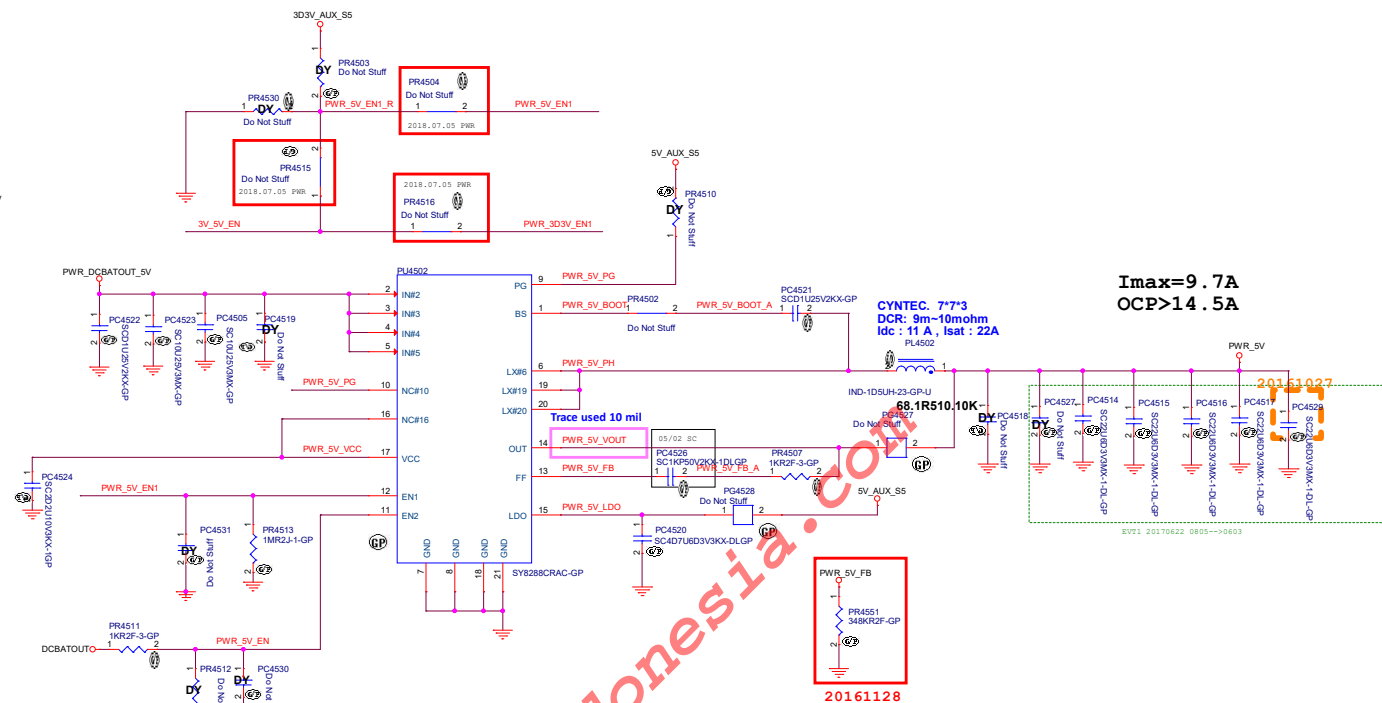




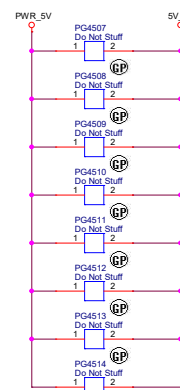
# SSID = PWR.Plane.Regulator\_5V



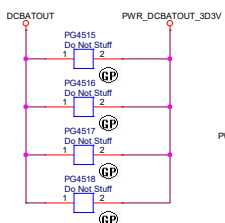
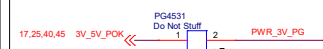
EN rat i ng 25V  
EN Rising Threshold : 0.8V  
Ilimit : 8A



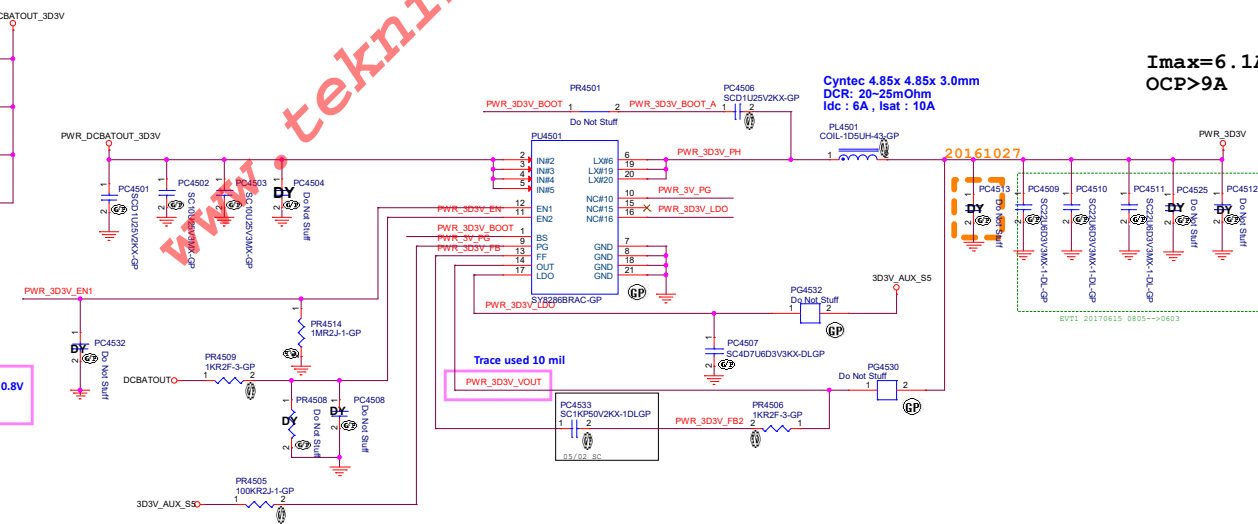
I<sub>max</sub>=9.7A  
OCP>14.5A



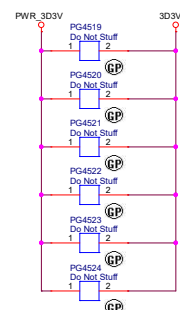
# SSID = PWR.Plane.Regulator\_3D3V



EN rat i ng 25V  
EN Rising Threshold : 0.8V  
Ilimit : 8A

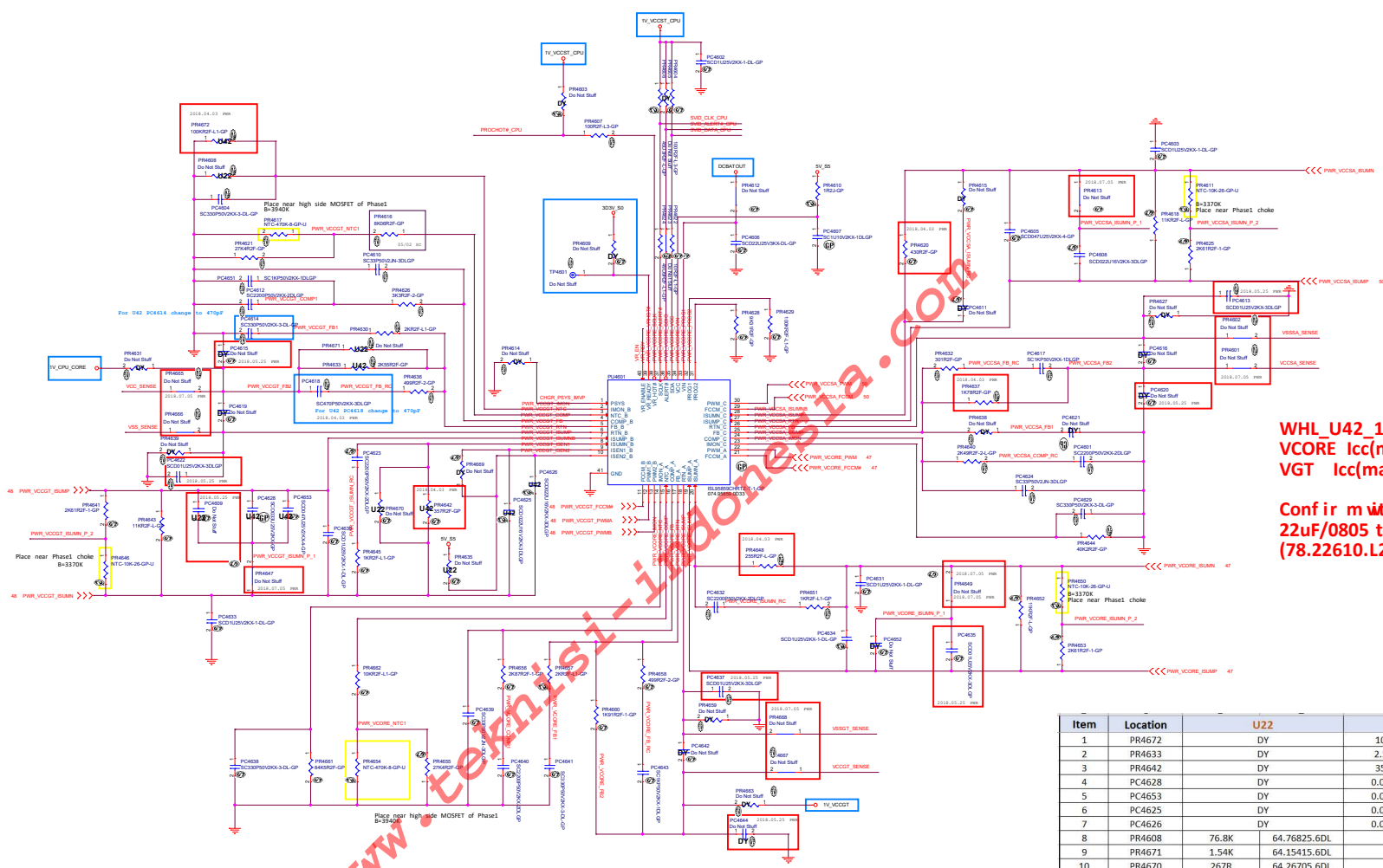


I<sub>max</sub>=6.1A  
OCP>9A



Main Func = CPU\_CORE

- 7 SWD\_CLK\_CPU <<<
- 7 SWD\_ALERTY\_CPU <<<
- 7 SWD\_DATA\_CPU <<<
- 7 VCC\_SENSE <<<
- 7 VSS\_SENSE <<<
- 48 PWR\_VCCST\_BEN1 >>>
- 48 PWR\_VCCST\_BEN2 >>>
- 8 VCCST\_SENSE <<<
- 8 VCCST\_SENSE <<<
- 8 VSSA\_SENSE <<<
- 8 VCCSA\_SENSE <<<
- 40 VL\_EN >>>
- 324,48 PRECHOTN\_CPU
- 44 CHGR\_PSYS\_BMP



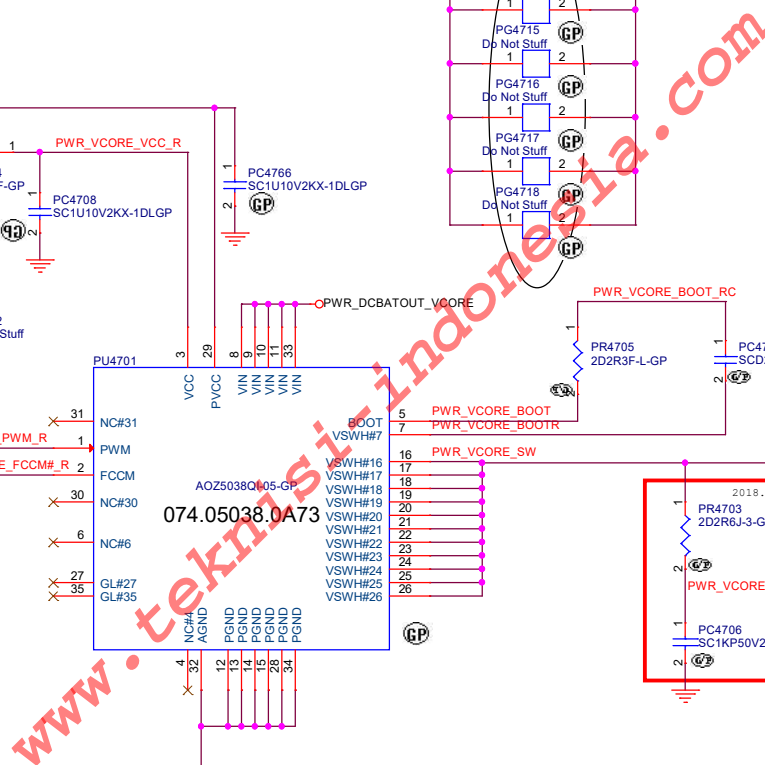
WHL\_U42\_15W  
VCORE Icc(max)=70A TDC=42 A  
VGT Icc(max)=31A TDC=18 A

Confir m at h EE  
22uF/0805 total 36pcs  
(78.22610.L2L)

Item	Location	U22		U42	
1	PR4672	DY		100K	64.10035.6DL
2	PR4633	DY		2.55K	64.25515.6DL
3	PR4642	DY		357R	64.35705.6DL
4	PC4628	DY		0.033u	78.33321.2FL
5	PC4653	DY		0.047u	078.47322.02FD
6	PC4625	DY		0.022u	78.22321.2FL
7	PC4626	DY		0.022u	78.22321.2FL
8	PR4608	76.8K	64.76825.6DL		DY
9	PR4671	1.54K	64.15415.6DL		DY
10	PR4670	267R	64.26705.6DL		DY
11	PR4635	1K	64.10015.6DL		DY
12	PC4609	0.01u	78.10322.2FLDL		DY
11	PC4618	1000p	78.10224.2FLDL	470p	78.47124.2FLDL
13	PU4802	DY		A0Z5038	074.05038.0073
14	PC4816	DY		10u	78.10612.58L
15	PC4817	DY		10u	78.10612.58L
16	PC4814	DY		10u	78.10612.58L
17	PC4815	DY		10u	78.10612.58L
18	PR4813	DY		2R2	64.2R205.6DL
19	PC4812	DY		1u	78.10523.5FLDL
20	PC4866	DY		1u	78.10523.5FLDL
21	PR4810	DY		2R2	64.2R205.55L
22	PC4811	DY		0.022u	78.22422.2BLDL
23	PL4802	DY		0.15uH	68.R1510.20A
24	PR4823	DY		100K	64.10035.6DL
25	PR4816	DY		3.65K	64.36515.6DL
26	PR4815	DY		10R	64.10R05.L1L
27	PR4821	DY		100K	64.10035.6DL
28	PT4803	DY		330u	79.33719.20C

5

**Main Func = CPU CORE**



Confirm with EE  
22uF/0805 total 33pcs  
(78.22610.L2L)

Cyntec 6.8mmx7.6mmx4.0mm  
DCR: 0.66m ohm +/-7%  
Idc : 36A , Isat : 45A

**PANASONIC**  
ESR: 9 mohm

BV UMA TC TPM

DELL

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title **NCP81382MN\_CPU\_VCORE(2/3)**

Size A3	Document Number <b>Bucky WHL</b>	Rev <b>SA</b>
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Date: Friday, July 13, 2018 Sheet 47 of 105



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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>NCP81210MN_CPU_VCCGTUS</b>			
Size A2	Document Number <b>Bucky WHL</b>	Rev <b>SA</b>	
Date: Friday, July 13, 2018		Sheet 49	of 106

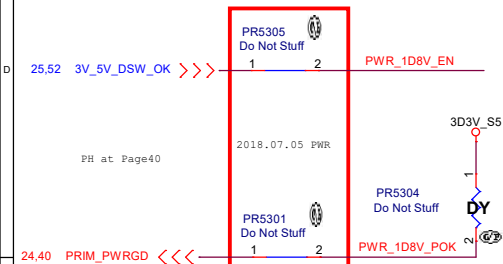




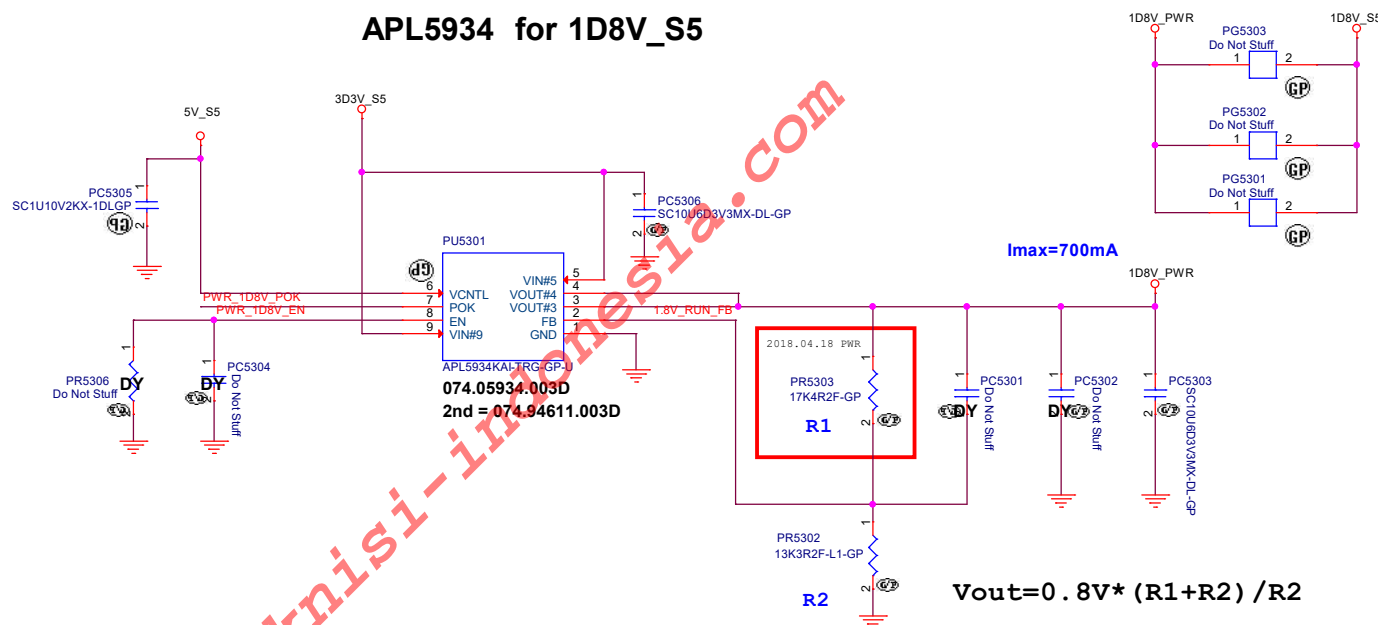




Main Func = 1D8V



## APL5934 for 1D8V\_S5



BV UMA TC TPM



Title			053_LDO-V1D8V&2D5V	
Size	Document	Number	Bucky WHL	
A3			Rev	SA
Date: Friday, July 13, 2018			Sheet	53 of 105

Main Func = 2D5V/ 1D8V

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Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

054\_LDO-V1D8V&2D5V

Size

A3

Document Number

Bucky WHL

Rev

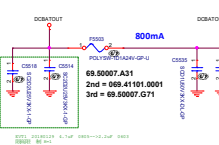
SA

Date: Friday, July 13, 2018

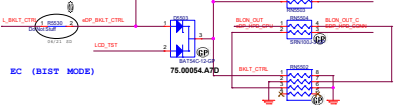
Sheet 54 of 105

Main Func = LCD

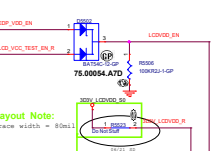
INVERTER POWER



Brightness

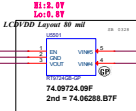


LCDVDD



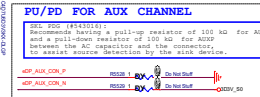
Layout Note:

Trace width = 80mil



Layout Note:

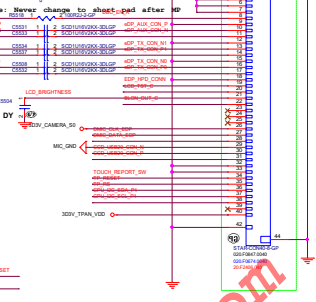
Trace width = 80mil



LCD

Camera

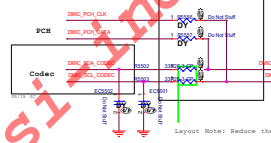
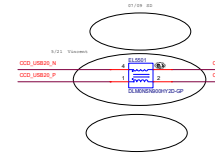
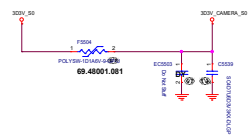
Touch Panel



Main Func = CAMERA

Follow Santa Fe reserved for modern standby

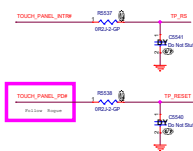
CAMERA POWER



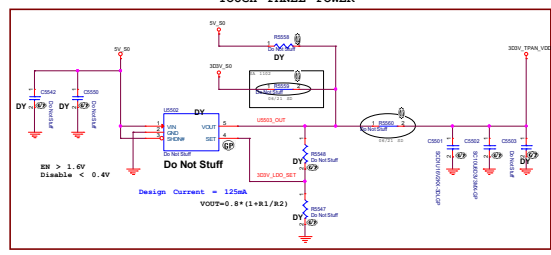
Layout Note: Reduce the stubs.

Main Func = Touch panel

Touch Panel




TOUCH PANEL POWER



Main Func = CRT

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Taipai Hsien 221, Taiwan, R.O.C.

Title

**CRT(Reserved)**

Size

A3

Document Number

**Bucky WHL**

Rev

**SA**

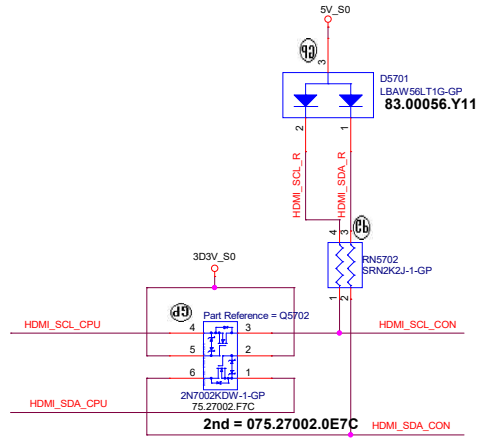
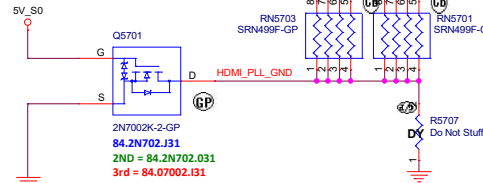
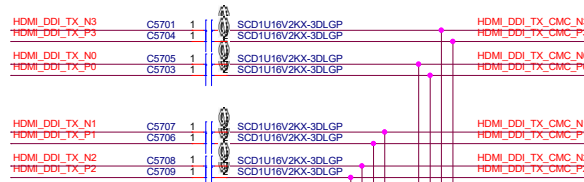
Date: Friday, July 13, 2018

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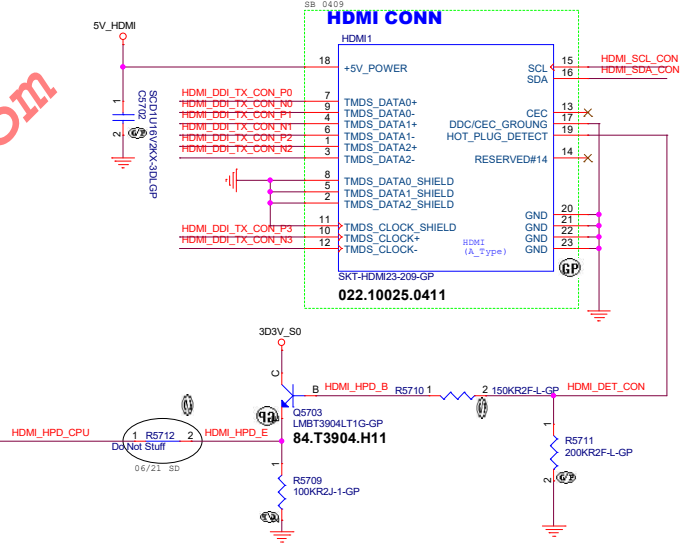
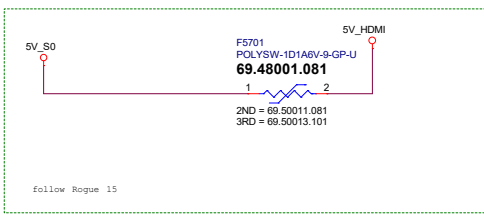
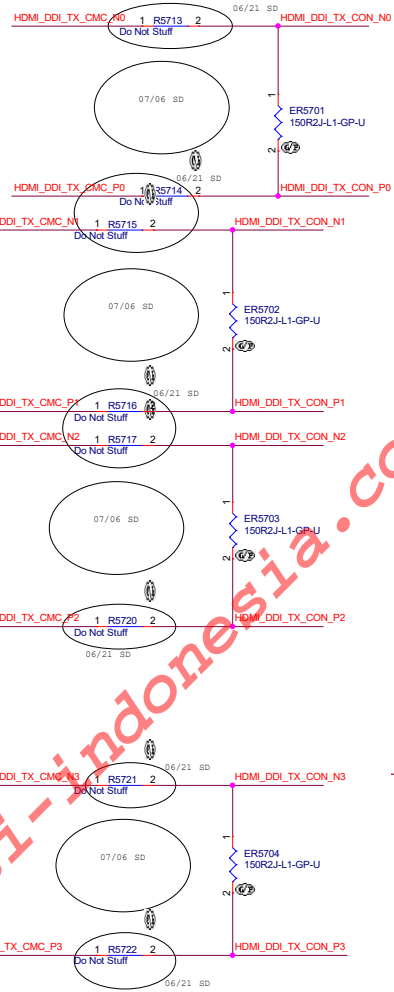
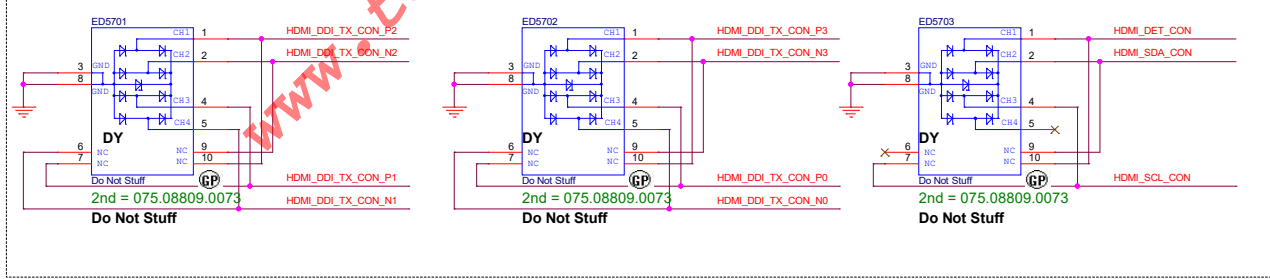
# SSID = HDMI Level Shifter/Connector

4 HDMI\_DDI\_TX\_N0  
4 HDMI\_DDI\_TX\_P0  
4 HDMI\_DDI\_TX\_N1  
4 HDMI\_DDI\_TX\_P1  
4 HDMI\_DDI\_TX\_N2  
4 HDMI\_DDI\_TX\_P2  
4 HDMI\_DDI\_TX\_N3  
4 HDMI\_DDI\_TX\_P3

4 HDMI\_SCL\_CPU  
4 HDMI\_SDA\_CPU  
4 HDMI\_HPD\_CPU



## EMI Request:




(Blanking)

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(Blanking)

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Taipei Hsien 221, Taiwan, R.O.C.

Title  
**(Reserved)**

Size  
A3

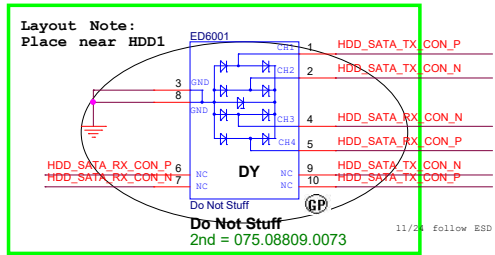
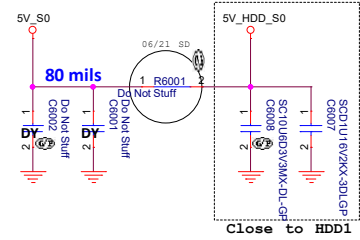
Document Number  
**Bucky WHL**

Rev  
**SA**

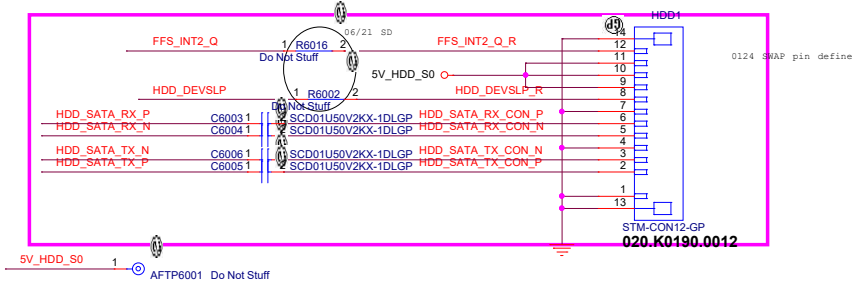
Date: Friday, July 13, 2018Sheet 59 of 105

Main Func = HDD

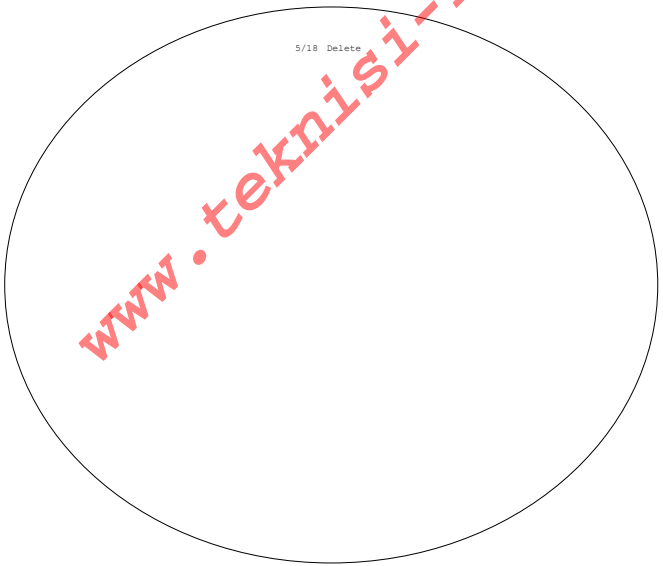
HDD



SATA HDD Connector



HDD Re-driver



BV UMA TC TPM

<b>DELL</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title <b>SATA IF HDD/ODD</b>			
Size	Document Number	Rev	
Custom	<b>Bucky WHL</b>	<b>SA</b>	
Date: Friday, July 13, 2018	Sheet 60 of 105		



**Main Func = WLAN**

## PCIE

```

16 WLAN_PCIE_TX_N    >>> _____
16 WLAN_PCIE_TX_P    >>> _____

16 WLAN_PCIE_RX_N    <<< _____
16 WLAN_PCIE_RX_P    <<< _____

```

## PCIE CLK

```

18 WLAN_CLK_CPU_N    >>> _____
18 WLAN_CLK_CPU_P    >>> _____
18,61 WLAN_CLKREQ_CPU_N <<< _____

```

USB2.0

16 BT\_USB20\_P << >> \_\_\_\_\_  
16 BT\_USB20\_N << >> \_\_\_\_\_

## Single end

```
21 BLUETOOTH_EN >>> _____
```

21	WIFI_RF_EN		
17,26,63,66,76,91	PLT_RST#		
18,24	SUS_CLK		

## Debug

24,68 HOST\_DEBUG\_TX >>

## Power EN (Madesimo)

17,24 AUX\_EN\_WOWL &gt;&gt;&gt;\_\_\_\_\_

18,61 WLAN\_CLKREQ\_CPU\_N &lt;&lt;&lt;—

```

19 BT_PCMOUT_CLKREQ0  >>> _____
19 BT_PCMFRM_CRF_RST_N  >>> _____

```

21 CNV\_WT\_DN0 >>> \_\_\_\_\_  
21 CNV\_WT\_DP0 >>> \_\_\_\_\_  
21 CNV\_WT\_DN1 >>> \_\_\_\_\_  
21 CNV\_WT\_DP1 >>> \_\_\_\_\_  
21 CNV\_WT\_CLKN >>> \_\_\_\_\_  
21 CNV\_WT\_CLKP >>> \_\_\_\_\_

```

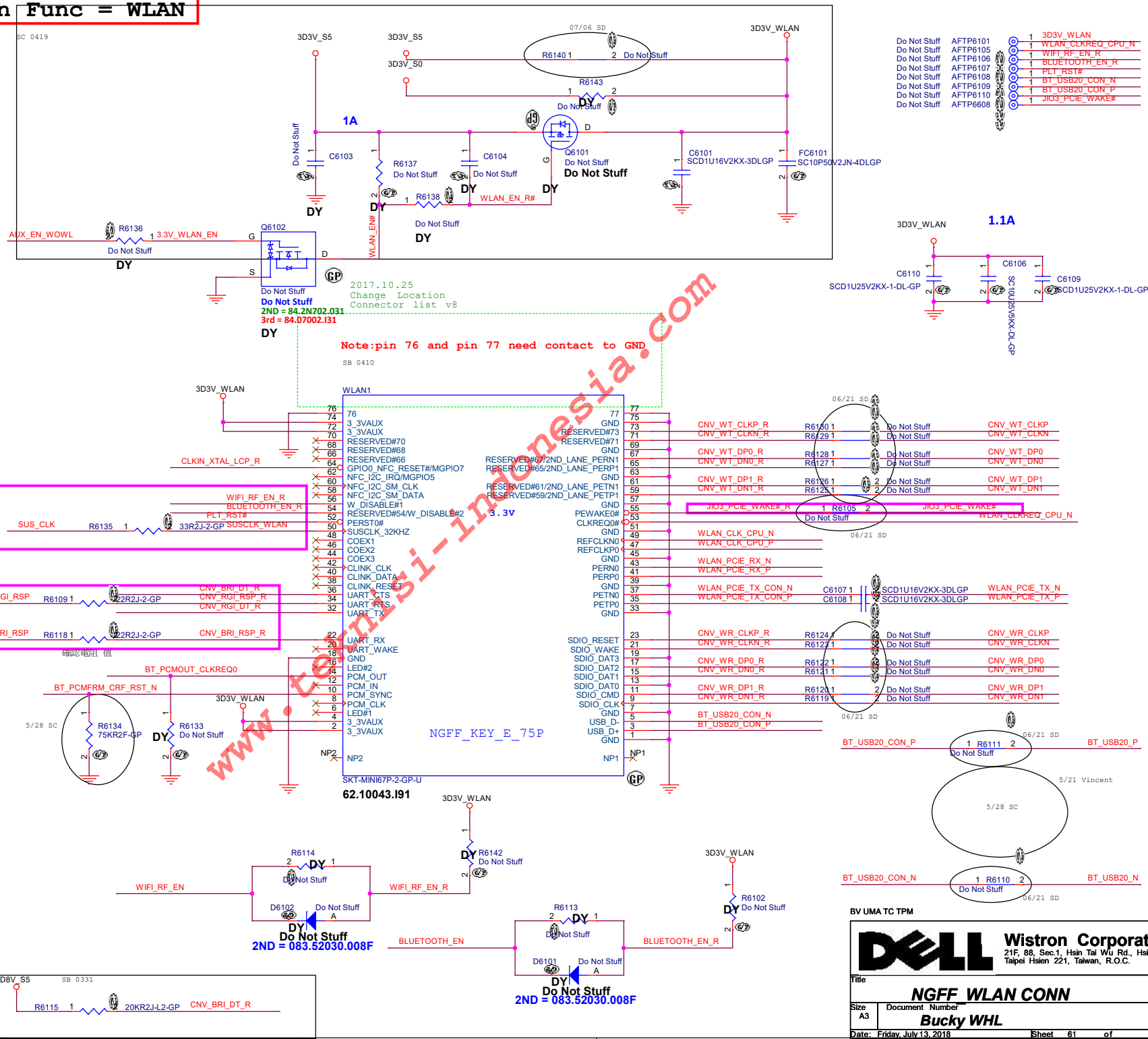
21 CNV_WR_DN0  <<<<_____
21 CNV_WR_DP0  <<<<_____
21 CNV_WR_DN1  <<<<_____
21 CNV_WR_DP1  <<<<_____
21 CNV_WR_CLKN <<<<_____
21 CNV_WR_CLKP <<<<_____

```

15,20 CNV\_RGI\_DT\_R >>> —  
20 CNV\_BRI\_DT\_R >>> —  
20 CNV\_BRI\_RSP <<< —  
20 CNV\_RGI\_RSP <<< —

18 JIO3\_PCIE\_WAKE#&gt;&gt;\_\_\_\_\_

18 CLKIN XTAL LCP R >>



(Blanking)

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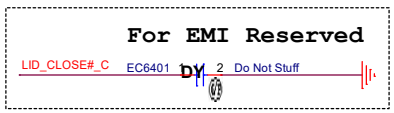
BV UMA TC TPM

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size A4	Document Number <b>Bucky WHL</b>		Rev <b>SA</b>
Date: Friday, July 13, 2018		Sheet 62 of	105



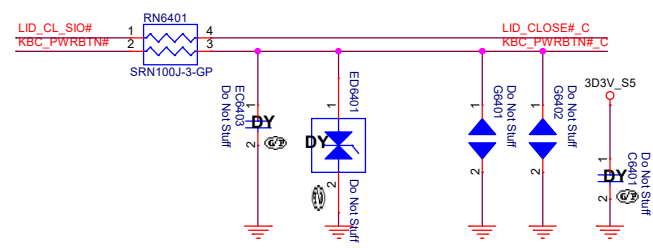
Main Func = Power BTN

Low activated from KBC GPIO



Power button

Layout note:  
G6401 place to bottom  
G6402 place to top

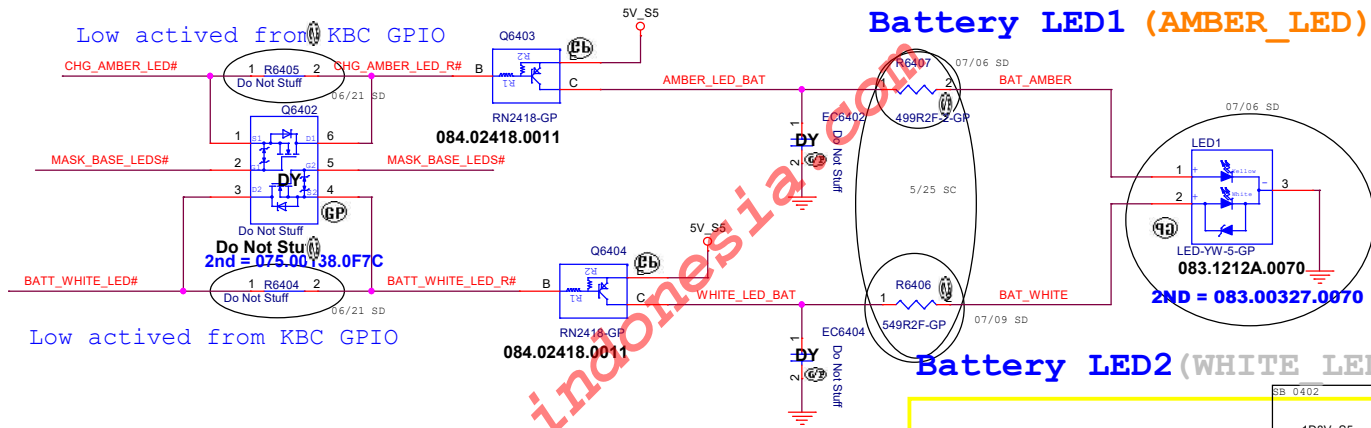


24 LID\_CL\_SIO# <<< \_\_\_\_\_  
24,68 KBC\_PWRBTN# <<< \_\_\_\_\_  
  
66 LID\_CLOSE#\_C >>> \_\_\_\_\_  
66 KBC\_PWRBTN#\_C <<< \_\_\_\_\_

Main Func = Battery LED

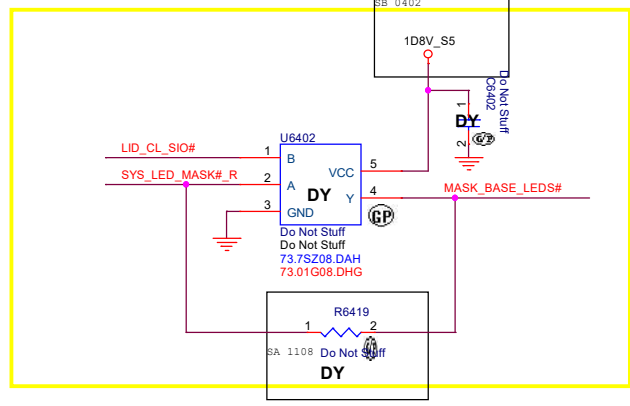
24 CHG\_AMBER\_LED# >>> \_\_\_\_\_  
  
24 SYS\_LED\_MASK#\_R >>> \_\_\_\_\_  
  
24 BATT\_WHITE\_LED# >>> \_\_\_\_\_

Low activated from KBC GPIO



Low activated from KBC GPIO

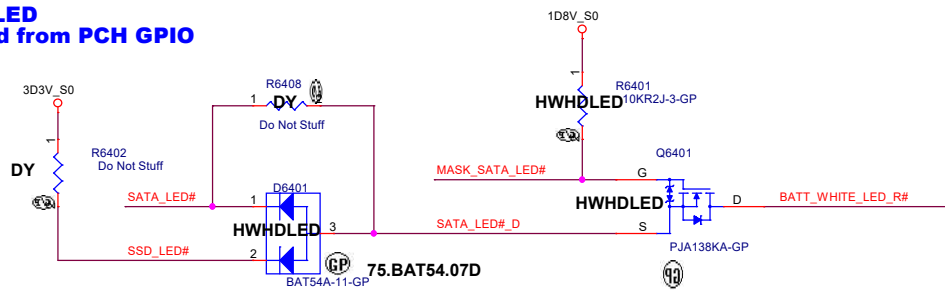
Battery LED2 (WHITE LED)



Main Func = HDD LED

24 MASK\_SATA\_LED# >>> \_\_\_\_\_  
  
16 SATA\_LED# >>> \_\_\_\_\_  
  
63 SSD\_LED# >>> \_\_\_\_\_

SATA HDD LED  
LOW activated from PCH GPIO

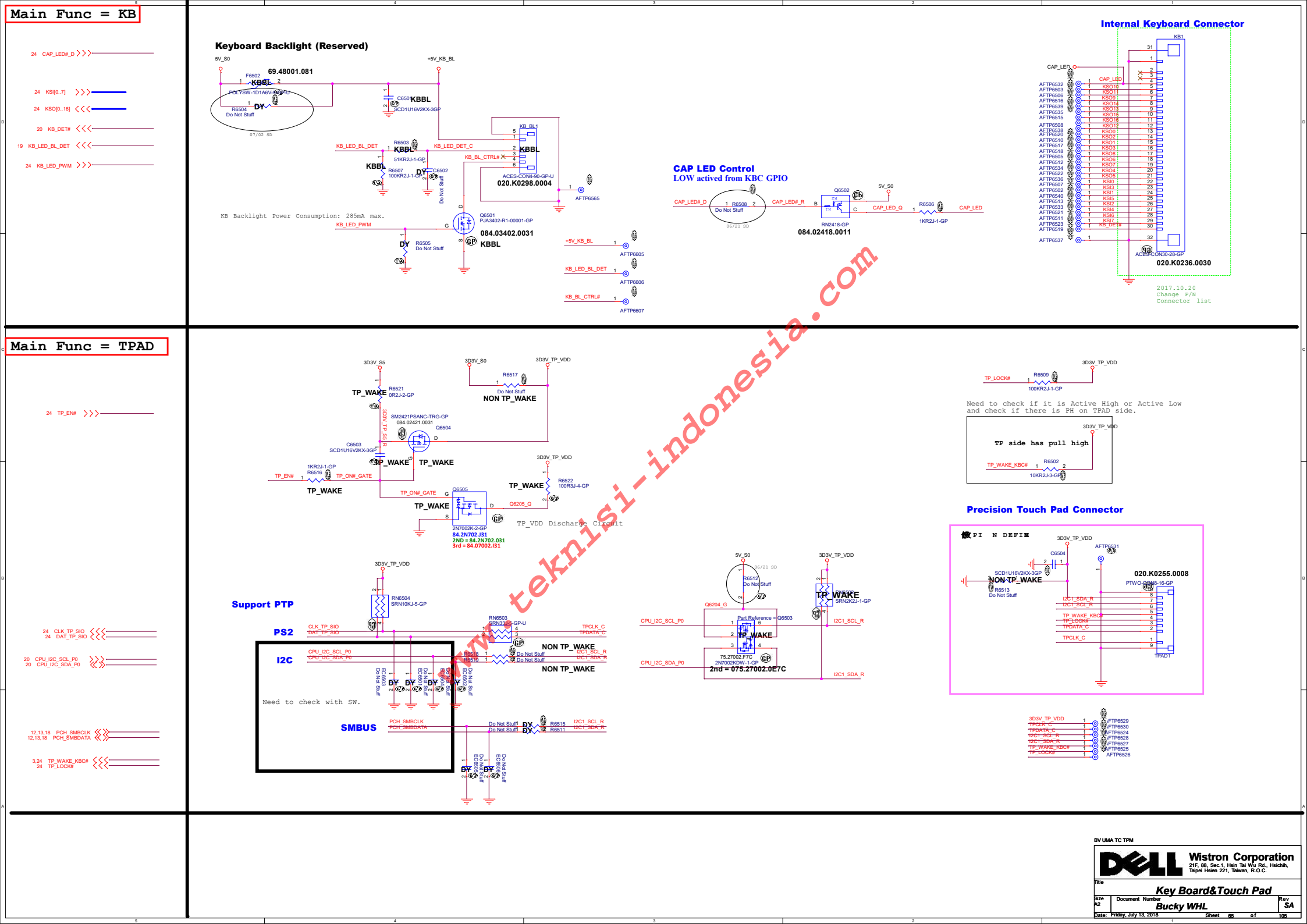


Add SSD LED function\_20170920

084.00138.0A31  
2nd = 084.00138.0C31

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<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>LED Board&amp;Power Button</b>			
Size A3	Document Number <b>Bucky WHL</b>	Rev <b>SA</b>	
Date: Friday, July 13, 2018	Sheet 64	of 105	



Main Func = IO Connector

I/O Board Connector

USB2.0

16 USB3\_USB20\_N <<<>>>  
16 USB3\_USB20\_P <<<>>>

Card Reder

16 CARD1\_USB20\_N <<>>  
16 CARD1\_USB20\_P <<>>

LAN

16 LAN\_PCIE\_RX\_N >>>  
16 LAN\_PCIE\_RX\_P >>>  
16 LAN\_PCIE\_TX\_N >>>  
16 LAN\_PCIE\_TX\_P >>>  
18 LAN\_CLK\_CPU\_N <<<  
18 LAN\_CLK\_CPU\_P <<<  
18 LAN\_CLKREQ\_CPU\_N <<< Edison 11/13 for STU  
24 PM\_LAN\_ENABLE >>>  
24 LANWAKE#\_IC >>>

FP

16 FP\_USB20\_N <<>>  
16 FP\_USB20\_P <<>>  
24 FPR\_SCAN# <<<

Free Fall Sensor

20,66,70 SENSOR\_I2C\_SCL <<>>  
20,66,70 SENSOR\_I2C\_SDA <<>>  
70 SENSOR\_I2C\_SCL\_2G <<>>  
70 SENSOR\_I2C\_SDA\_2G <<>>  
20 GSEN\_INT1 >>>  
20 GSEN\_INT2 >>>  
70 GSEN2\_INT1 >>>  
70 GSEN2\_INT2 >>>

17,26,61,63,76,91 PLT\_RST# >>>

20,66,70 SENSOR\_I2C\_SDA <<>>  
20,66,70 SENSOR\_I2C\_SCL <<>>

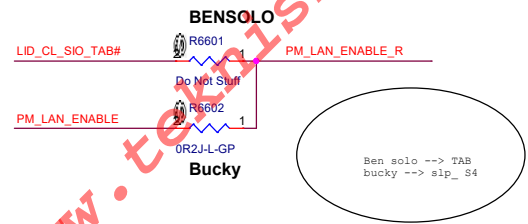
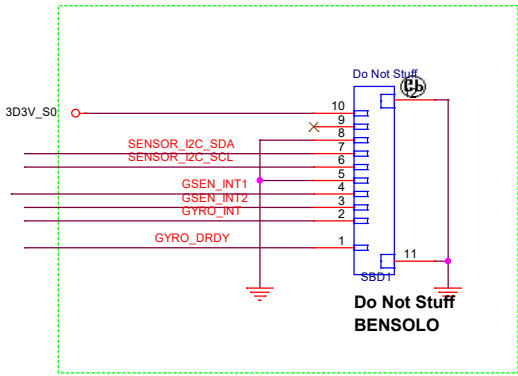
70 GYRO\_INT >>>  
20 GYRO\_DRDY >>>

24 LID\_CL\_SIO\_TAB# <<<  
64 LID\_CLOSE#\_C >>>  
64 KBC\_PWRBTN#\_C <<<

17,40,51,68 PM\_SLP\_S4# >>>

Sensor Board Connector

2017.10.20  
Change P/N  
Connector list



Pitch: 1mm  
Power: 6 pins  
GND: 5 pins

Wire

FP

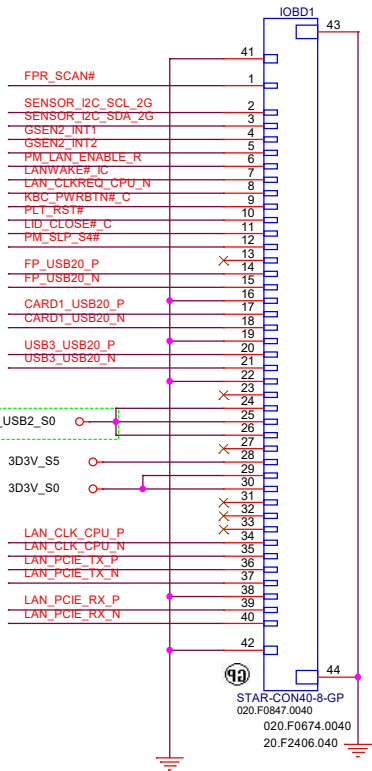
Card Reader

USB2.0 port 3

2017.10.25  
Modify netname  
follow STD

FP /Card Reder power  
EVR1 20170628 FP vendor use +3.3V

Coaxial



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application without get Wistron permission

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Title: <b>IO Board Connector</b>			
Size: A3	Document Number: <b>Bucky WHL</b>	Rev: <b>SA</b>	
Date: Friday, July 13, 2018		Sheet: 66	of: 105

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Title

**Free Fall Sensor**

Size  
A3

Document Number

**Bucky WHL**

Rev  
SA

Date: Friday, July 13, 2018

Sheet 67 of 105

# Main Func = Debug

## ESPI

18,24 ESPI\_CLK >>>  
18,24 ESPI\_RESET# >>>  
18,24 ESPI\_CS# >>>

18,24 ESPI\_IO[3..0] <<<  
ESPI\_IO3  
ESPI\_IO2  
ESPI\_IO1  
ESPI\_IO0

## UART

24 HOST\_DEBUG\_TX >>>  
20 UART\_2\_CTXD\_DRXD >>>  
20 UART\_2\_CRXD\_DTXD <<<

## APS

18 RTC\_RST# >>>  
24,64 KBC\_PWRBTN# >>>  
17,27,40 PM\_SLP\_S3# >>>  
17 PM\_SLP\_S5# >>>  
17,40,51,66 PM\_SLP\_S4# >>>  
17 SIO\_SLP\_A# >>>  
17,24,40,91 PM\_SLP\_S0# >>>  
17 XDP\_DBRESET# >>>

Modify\_21070802

3D3V\_S0

HOST\_DEBUG\_TX R6801 1

2 Do Not Stuff

HOST\_DEBUG\_TX\_CON

UART\_2\_CTXD\_DRXD R6802 1

Do Not Stuff

UART\_2\_CTXD\_DRXD\_CON

UART\_2\_CRXD\_DTXD R6803 1

Do Not Stuff

UART\_2\_CRXD\_DTXD\_CON

PM\_SLP\_S3#1 TP9952 Do Not Stuff

PM\_SLP\_S5#1 TP9949 Do Not Stuff

PM\_SLP\_S4#1 TP9950 Do Not Stuff

SIO\_SLP\_A# 1 TP9951 Do Not Stuff

RTC\_RST# 1 TP9953 Do Not Stuff

KBC\_PWRBTN# 1 TP9954 Do Not Stuff

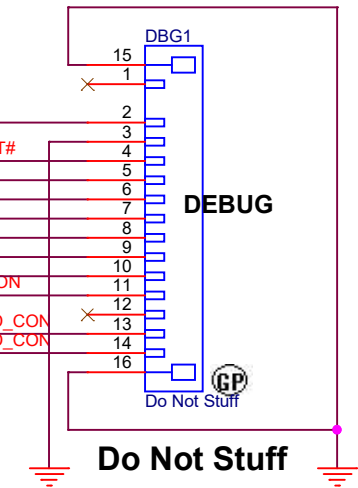
PM\_SLP\_S0# 1 TP9956 Do Not Stuff

XDP\_DBRESET# 1 TP9955 Do Not Stuff

EC6801

Do Not Stuff

## ESPI Debug Connector



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Title

Dubug connector

Size  
A4

Document Number

Bucky WHL

Rev  
SA

Date: Friday, July 13, 2018

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SSID = User.interface

```
66 GSEN2_INT1 <<< _____
66 GSEN2_INT2 <<< _____

20 GSEN2_INT1_C <<< _____
20 GSEN2_INT2_C <<< _____

18 FFS_INT1 <<< _____

20,66 SENSOR_I2C_SCL << _____
20,66 SENSOR_I2C_SDA << _____
66 SENSOR_I2C_SCL_2G << _____
66 SENSOR_I2C_SDA_2G << _____
20 GYRO_INT_C <<< _____

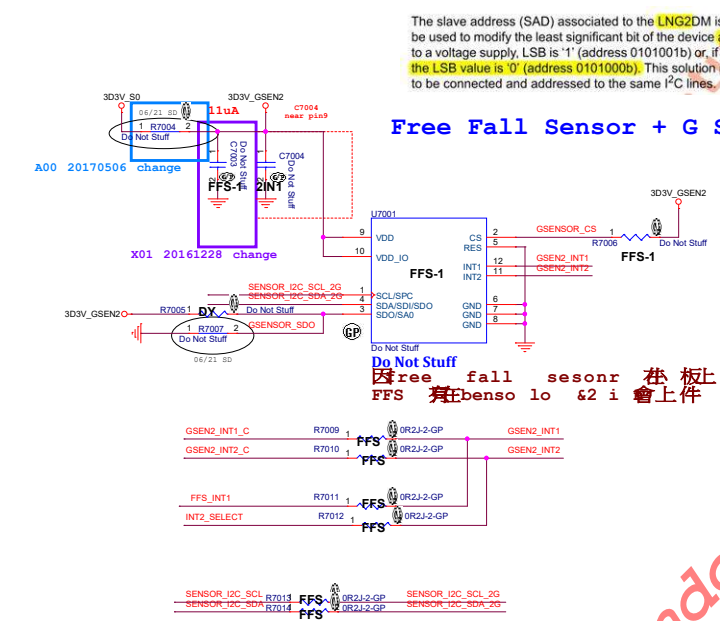
20 FFS_INT2 <<< _____

66 GYRO_INT >>> _____

60 FFS_INT2_Q <<< _____
```

# Free Fall Sensor

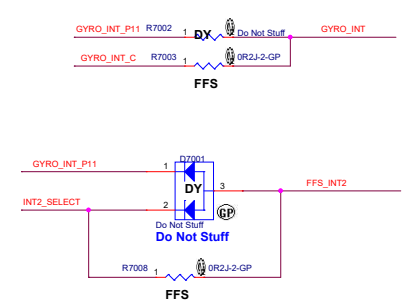
ref KR13\_20170801  
Reserve FFS-1



## Free Fall Sensor + G Sensor

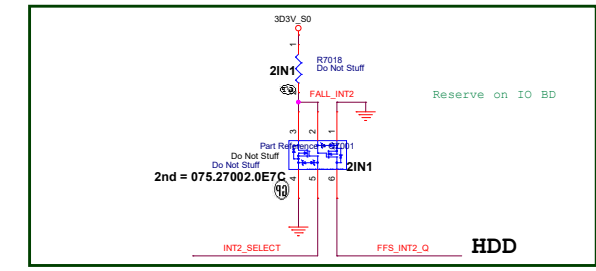
Free fall sensor 在板上,所以 E-1 在  
Benso lo & i 會上件

## combine G



Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



Note:

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

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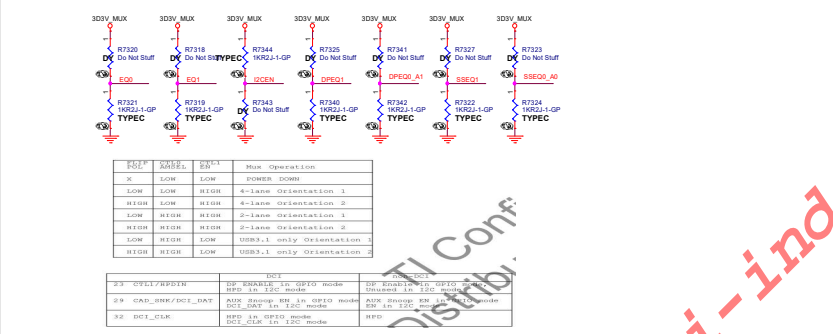
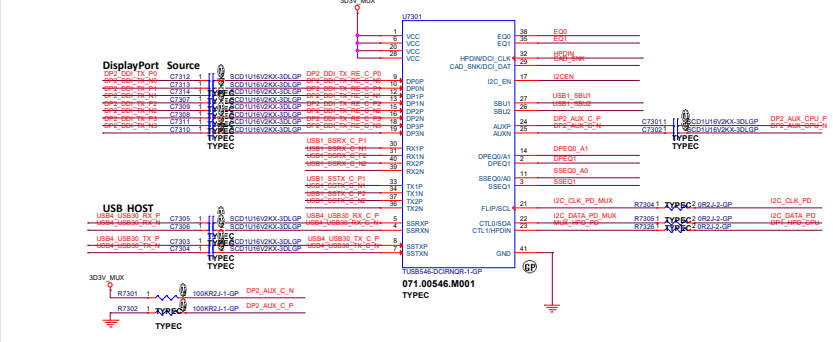
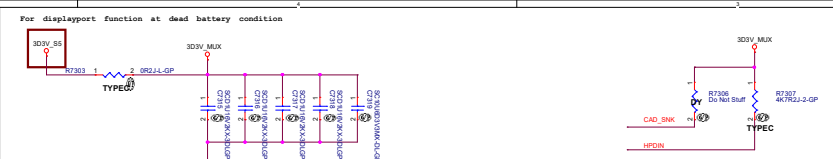


Main Func = TYPEC MUX

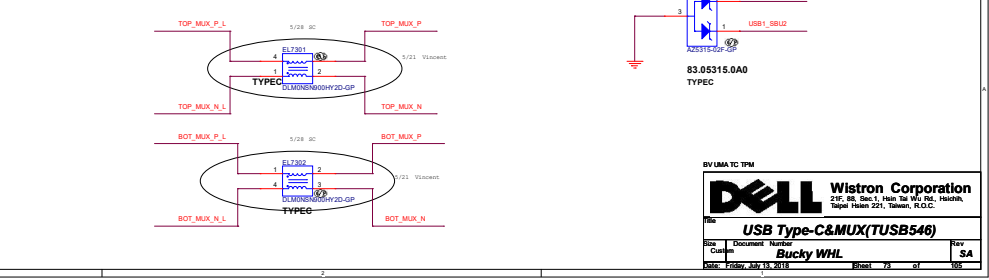
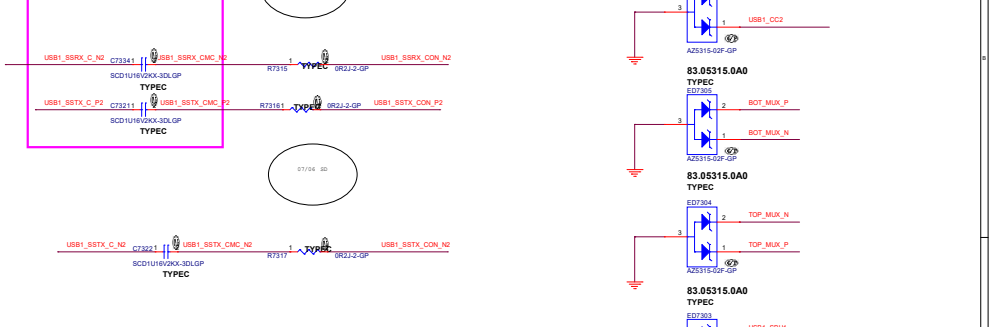
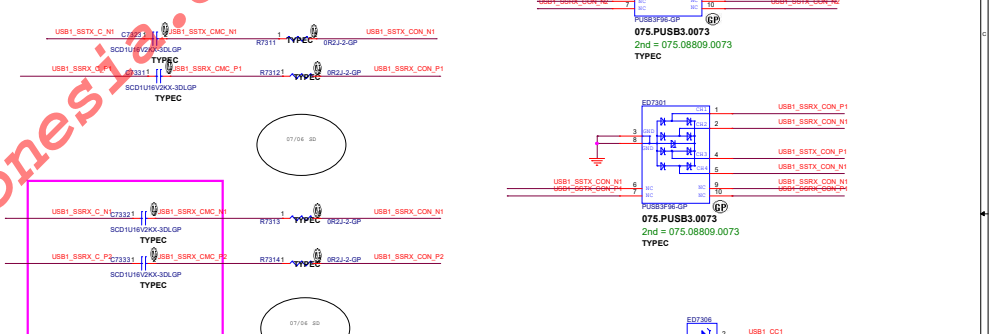
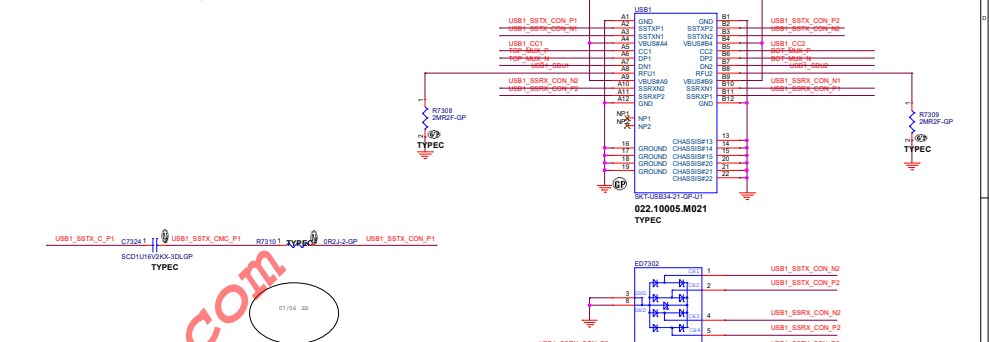
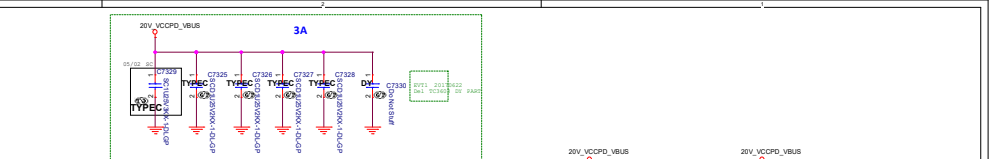


I2C/USB MUX

TypeC CC



IO#	NAME	IO#	NAME	IO#	NAME
1	DP2_D0+	2	DP2_D0-	3	DP2_D1+
4	DP2_D1-	5	DP2_D2+	6	DP2_D2-
7	DP2_D3+	8	DP2_D3-	9	DP2_AUX_CPU_P
10	DP2_AUX_CPU_N	11	DP2_AUX_CPU_P	12	DP2_AUX_CPU_N






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A3

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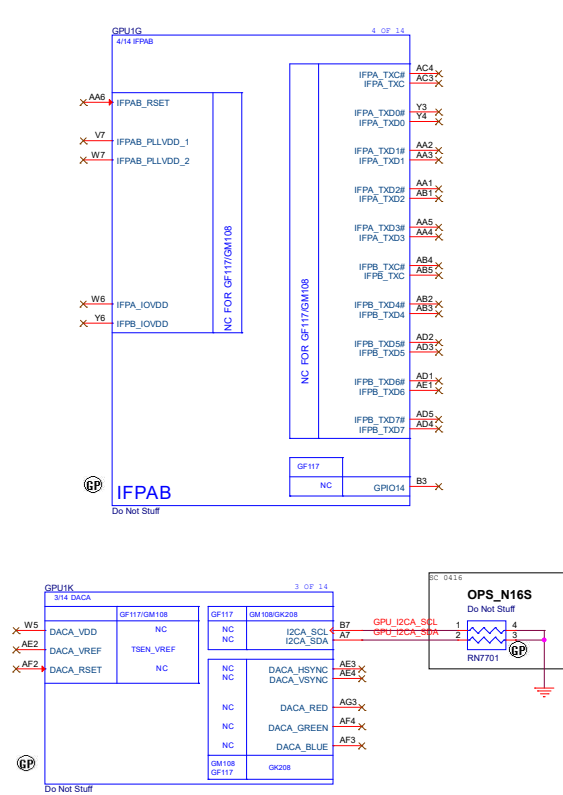
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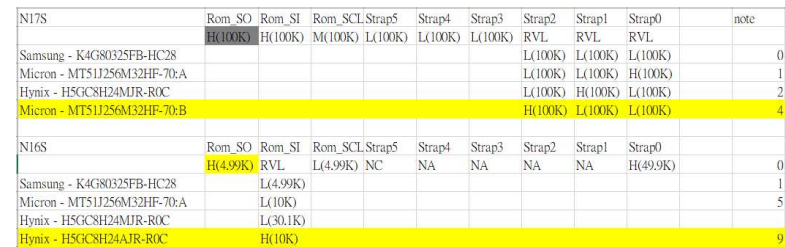






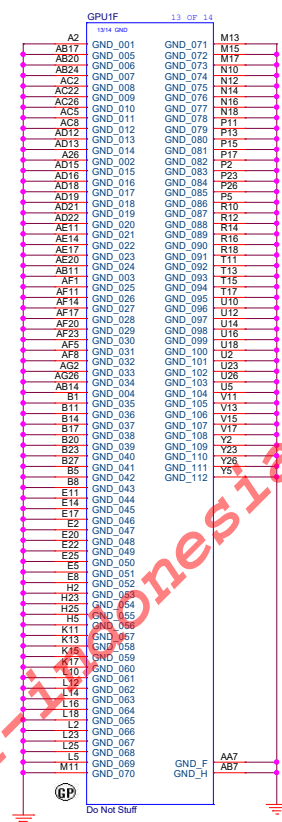
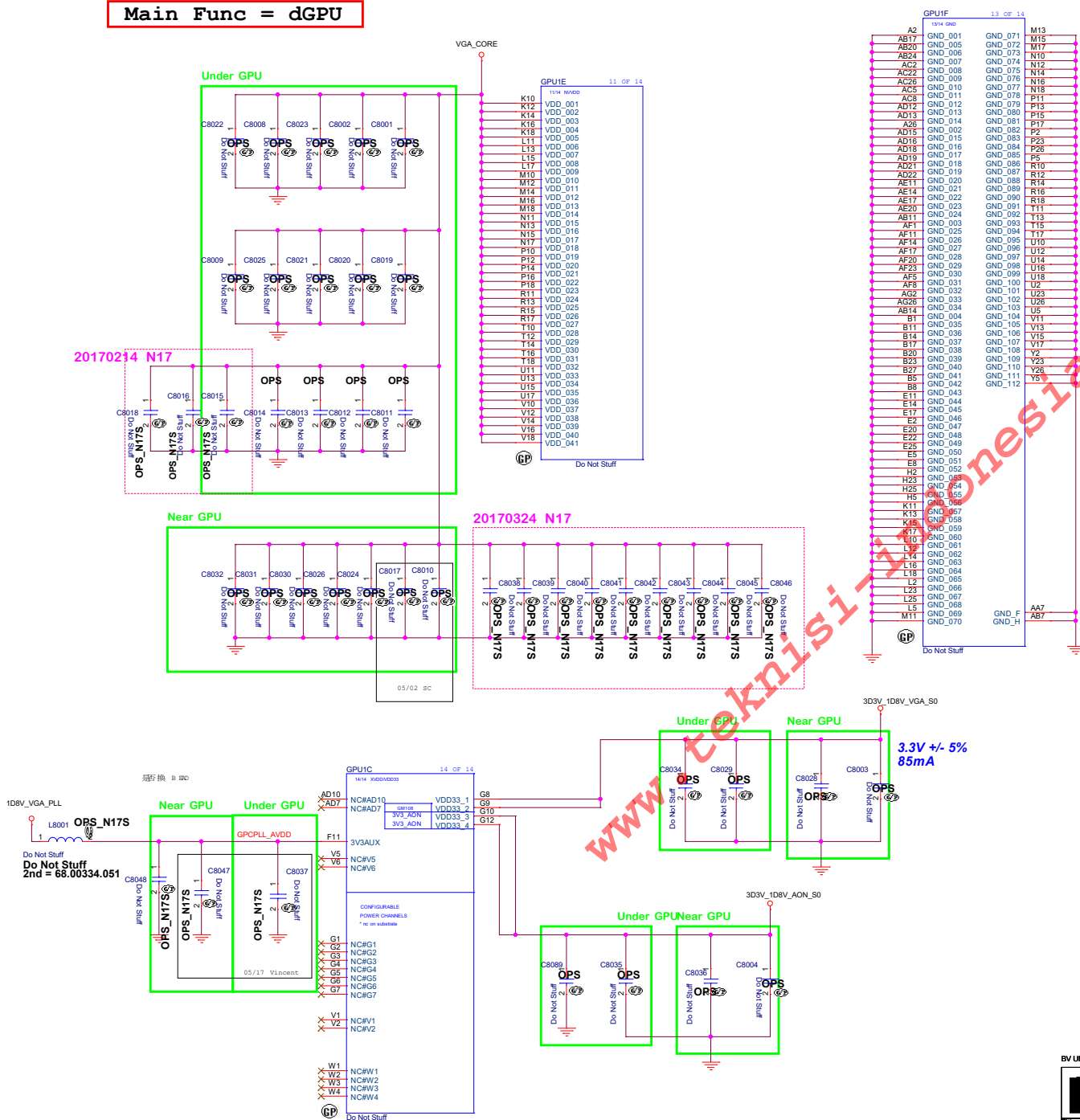
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<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd, Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.	
File			
<b>GPU(4/5)GPIO/STRAP</b>			
Size Custom Document Number			Rev
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**Main Func = dGPU**

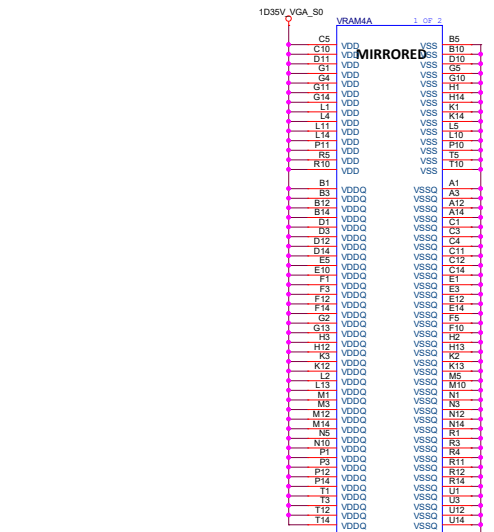
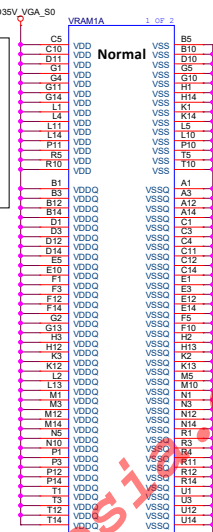
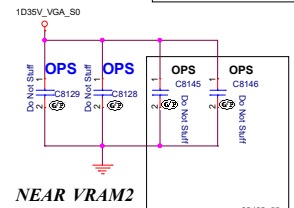
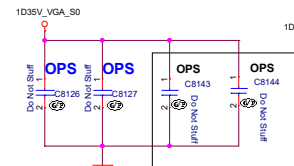
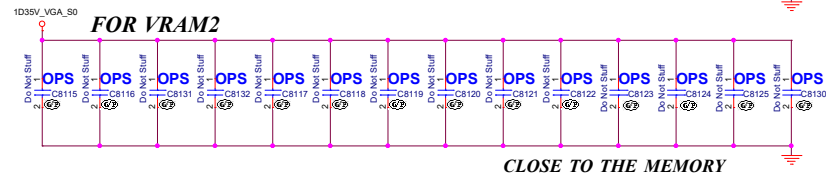
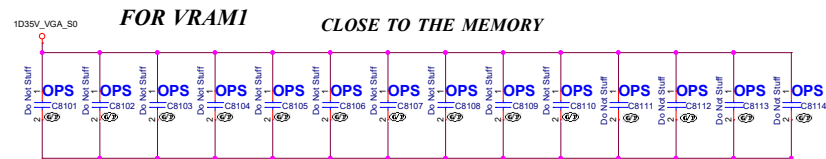


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Title				<b>GPU(5/5)PWR/GND</b>			
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SSID = VRAM



Place close VDD ball

Place close VDD ball

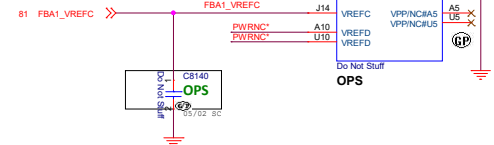
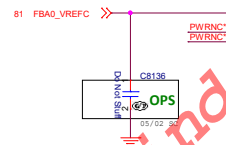
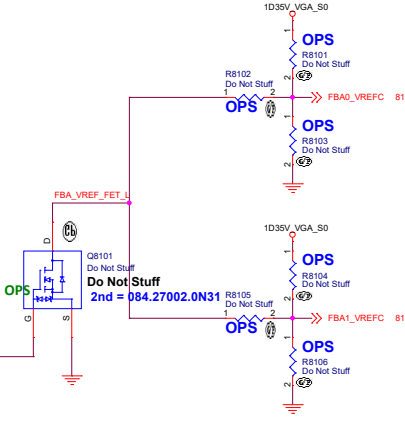
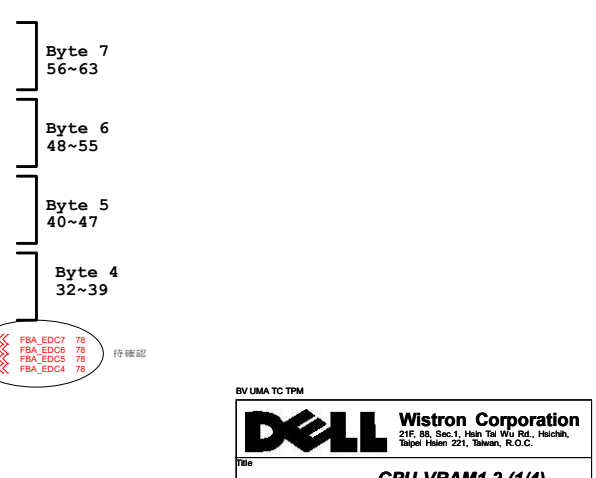
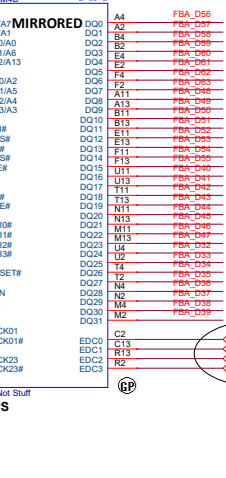
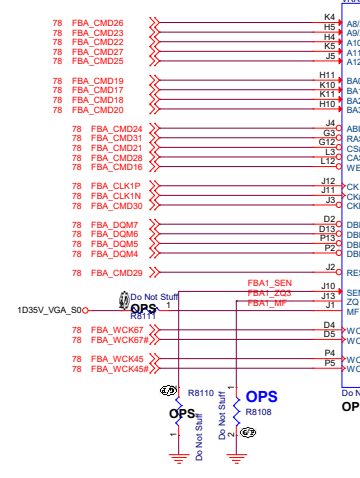
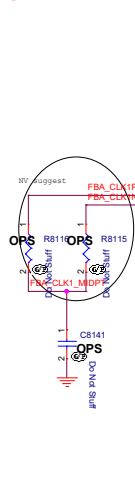
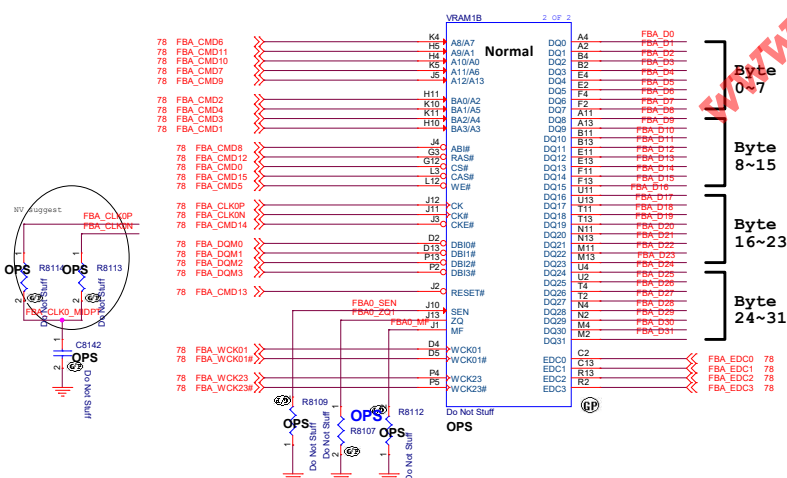


TABLE GDDR5 VIDEO MEMORY 072.05424.0A0U 072.44132.000U 072.04032.000N

	HYNIX 4GBITS (128Mx32)	SAMSUNG 4GBITS (128Mx32)	Micron 4GBITS (128Mx32)
VRAM1			
VRAM2	H5GC4H24AJR-T2C	K4G41325FC-HC03	EDW4032BAGB-60-F-D




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Main Func = dGPU

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**GPU-VRAM5,6 (3/4)**

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A3

Document Number

Rev  
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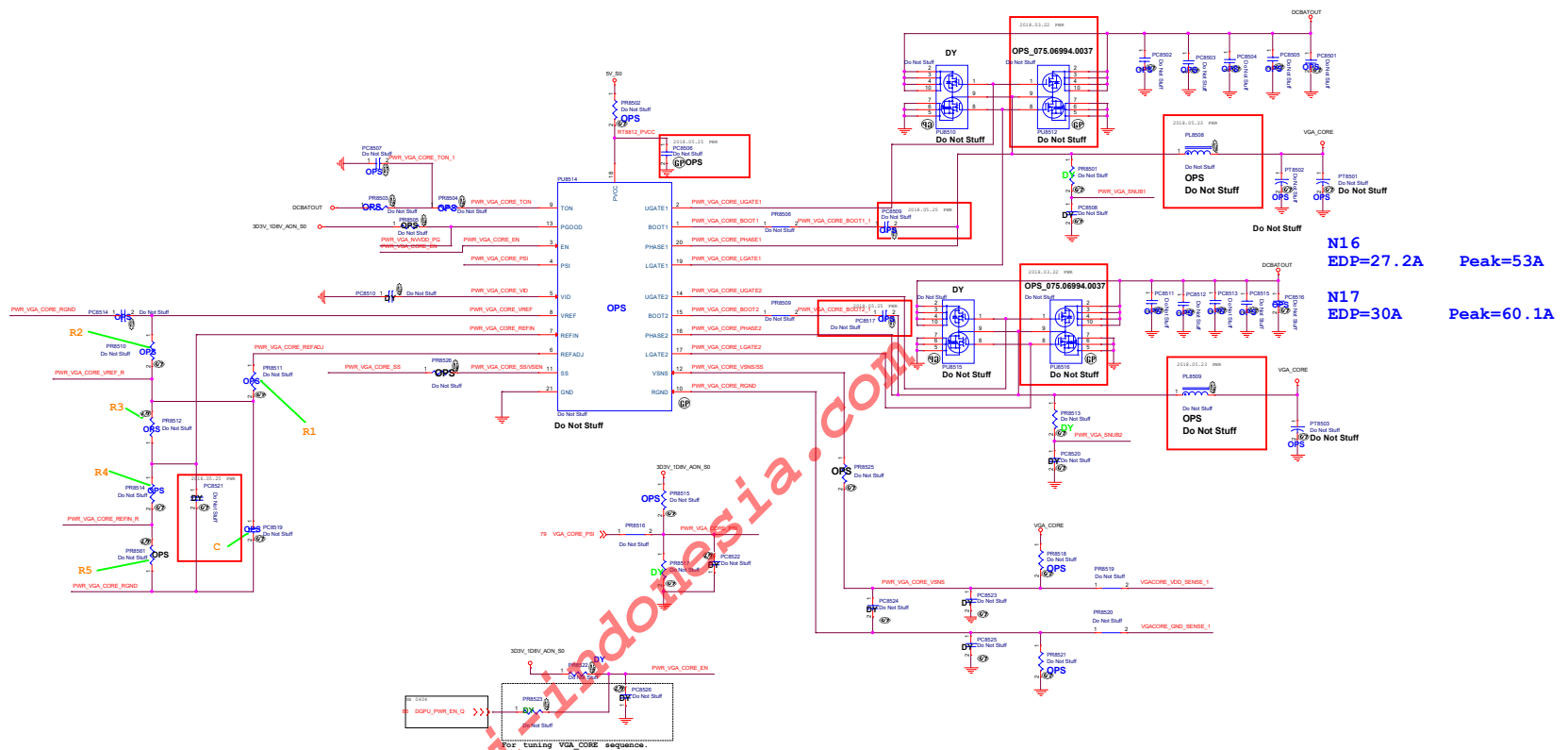
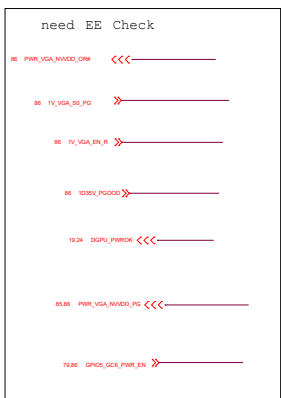
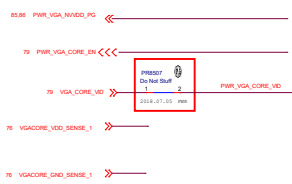
Sheet 83 of 105

Main Func = dGPU

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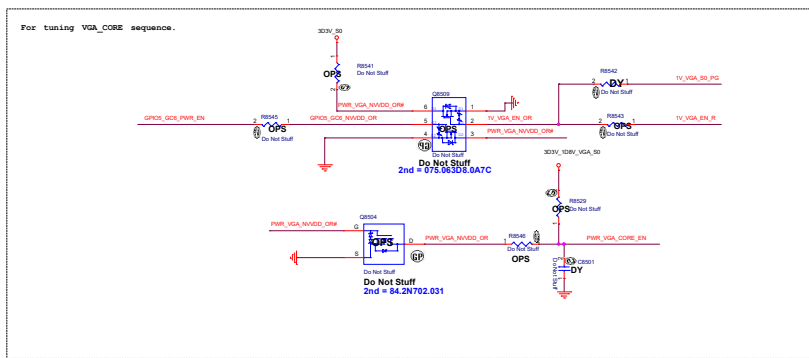
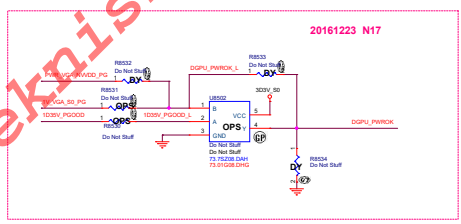


Main Func = dgFX\_CORE

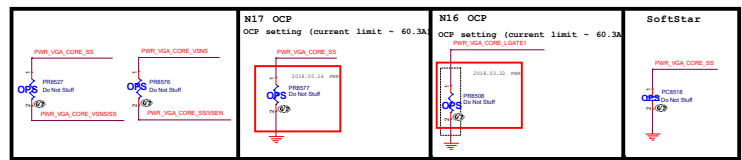


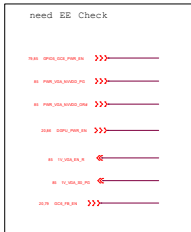
N16  
EDP=27.2A Peak=53A

N17  
EDP=30A Peak=60.1A



Item	Location	N16	N17
1	PUR514	RT8812AGQW 74.08812.073	RT8816AGQW 074.08816.0A73
2	PR8511	20K 64.20025.6DL	6.19K 64.61915.6DL
3	PR8510	20K 64.20025.6DL	20.5K 64.20525.6DL
4	PR8512	2K 64.20015.6DL	4.32k 64.43215.6DL
5	PR8514	18K 64.18025.6DL	16.5K 64.16525.6DL
6	PR8561	OR 63.R0034.1DL	309R 64.30905.6DL
7	PC8519	2700p 78.27224.2FLDL	4700p 078.47222.02FD
8	PR8525	OR 63.R0034.1DL	
9	PR8526	OR 63.R0034.1DL	
10	PR8527	DY	OR 63.R0034.1DL
11	PR8576	DY	OR 63.R0034.1DL
12	PR8577	DY	160K 64.16035.6DL
13	PR8508	15.4K 64.15425.6DL	DY
14	PR8504	348K 64.34835.6DL	499K 64.49935.6DL

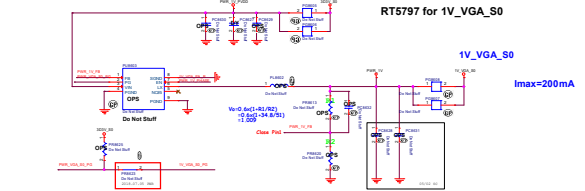
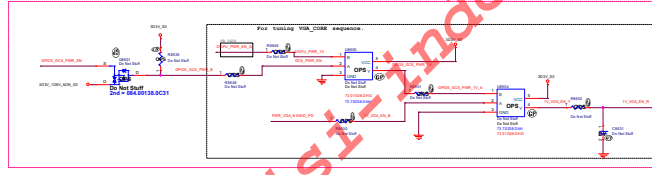
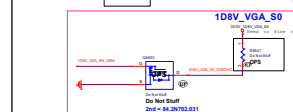
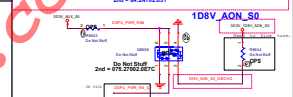
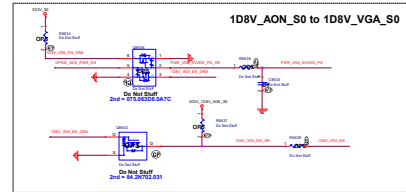
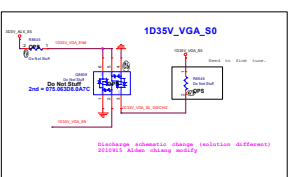
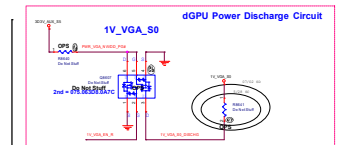
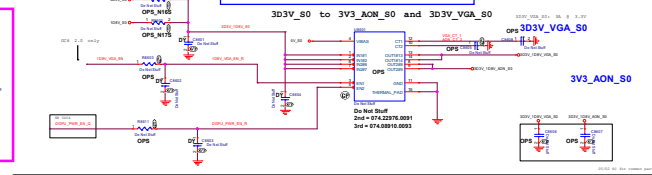
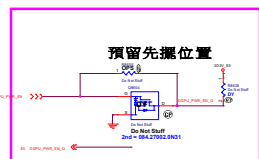




PARAMETER	MIN	MAX	UNITS
VIN1.2 Input voltage range	3.0	Vmax	V
VBIAS Bias voltage range	2.5	5.5	V
EN1.2 ON voltage range	0	5.5	V
VSOUT1.2 Output voltage range	---	VIN1.2	V
VIN High-level input voltage, EN1, EN2	1.2	5.5	V
VL Low-level input voltage, EN1, EN2	---	0.5	V
CT1.2 Input Capacitor	1	---	$\mu F$

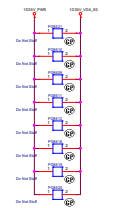
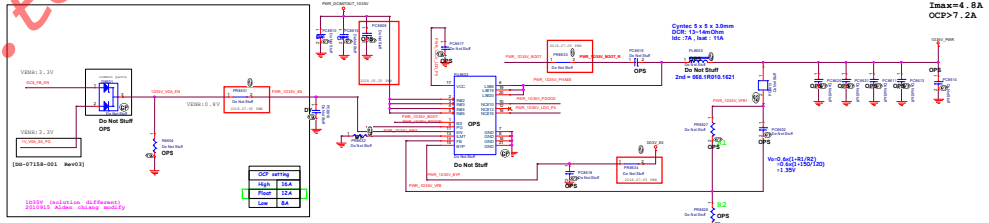
Main Func = dGPU G5516 for 1.8V\_AON\_S0

Main Func = dGPU



1D35V\_VGA\_S0

SY8288RAC for 1D35V



Main Func = dGPU

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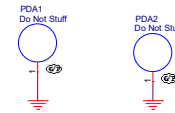
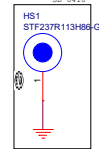
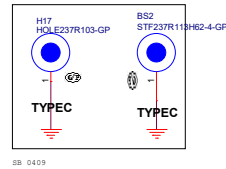
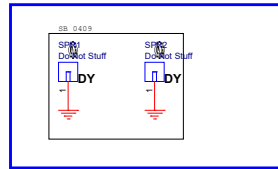
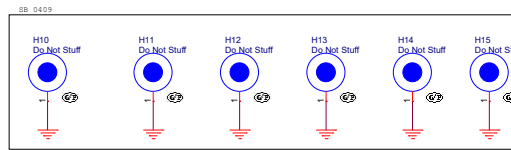
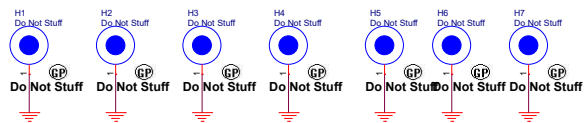
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A4	<b>Bucky WHL</b>	<b>SA</b>		
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## Main Func = UnusedParts

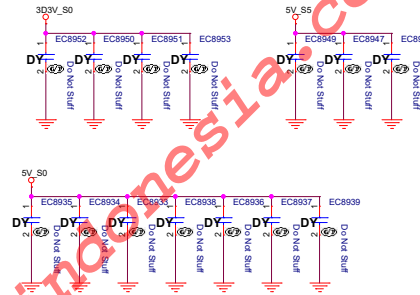
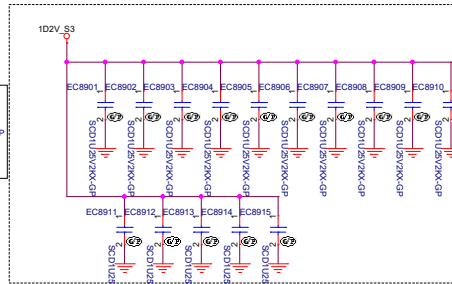
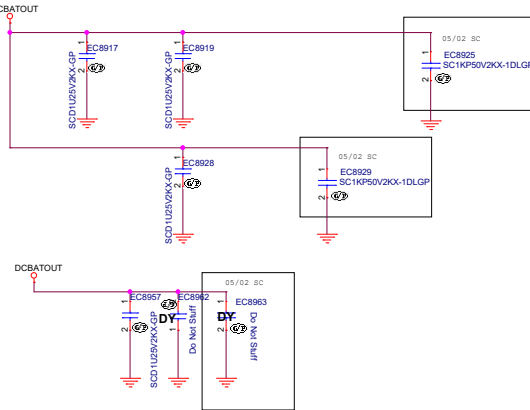


For acoustic noise

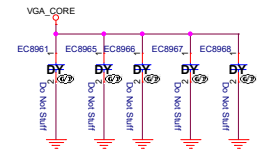
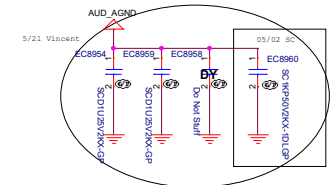


## Main Func = EMI Capacitors

Mind the voltage rating of the caps.

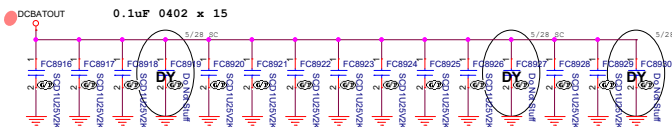
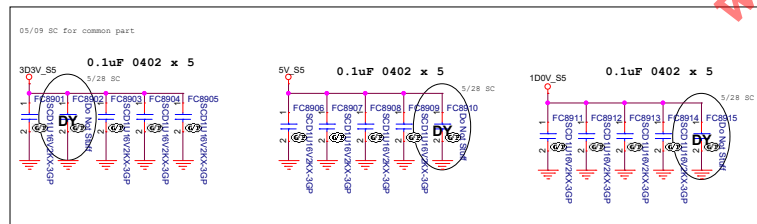


remove 1d5V\_VGA\_S0 EC CAP\_21070719



## Main Func = RF Capacitors

For RF solution RFQ 2017/08/11 Mind the voltage rating of the caps.



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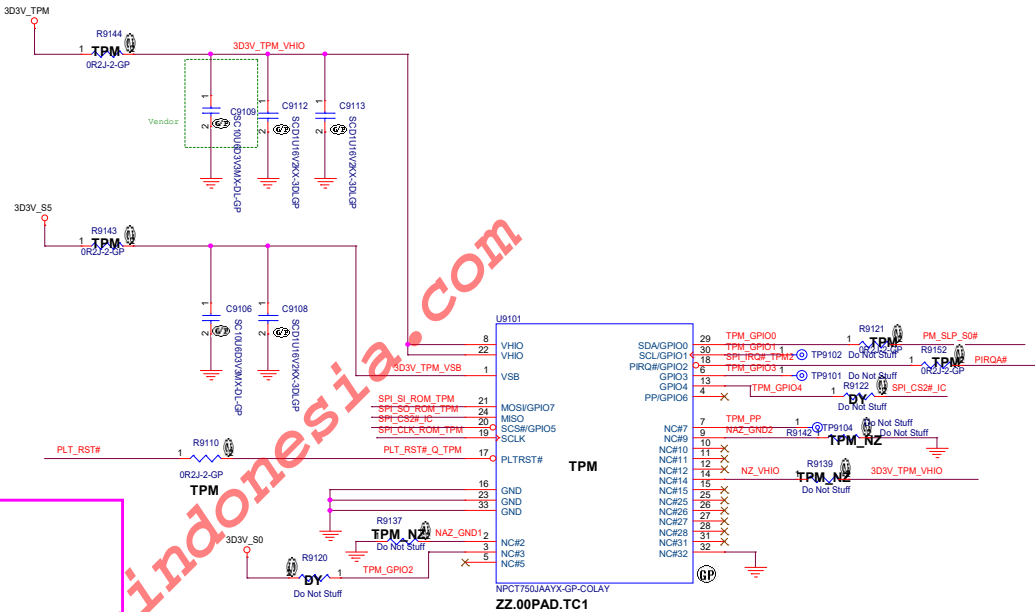
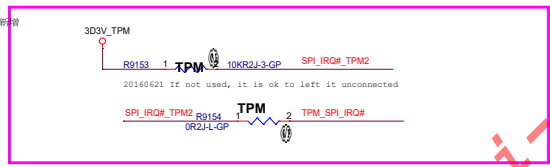
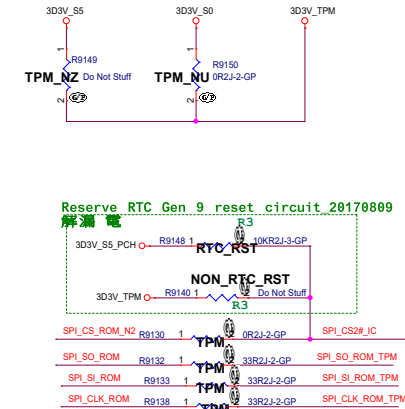
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<b>Reserved</b>			
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SSID = TPM

Change to use co-lay TP750X & Z32H330 follow DT project\_20170921

18,25 SPI\_SO\_ROM <<< \_\_\_\_\_  
15,18,25 SPI\_SI\_ROM >>> \_\_\_\_\_  
18,25 SPI\_CLK\_ROM >>> \_\_\_\_\_  
18 SPI\_CS\_ROM\_N2 >>> \_\_\_\_\_  
  
17,26,61,63,66,76 PLT\_RST# >>> \_\_\_\_\_  
  
20 PIRQA# <<< \_\_\_\_\_  
18 TPM\_SPI\_IRQ# <<< \_\_\_\_\_  
17,24,40,68 PM\_SLP\_S0# >>> \_\_\_\_\_



NU: Nuvoton TPM :071.00750.0003  
NZ: NationZ TPM :071.32330.0003

TPM\_ID at P.19

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File		TPM2.0	
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SSID = Finger Print

PWFPR(Botton side finger Print Sensor)

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Title <b>(Reserved)</b>			
Size A4	Document Number <b>Bucky WHL</b>		Rev <b>SA</b>
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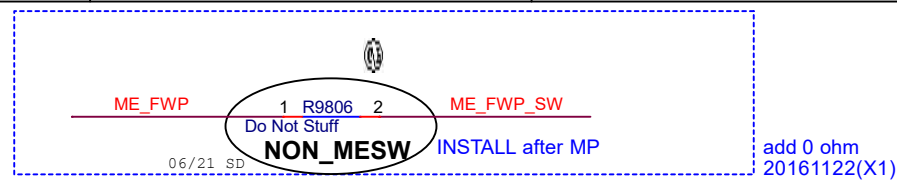
(Blanking)

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Title			
LVDS_Switch			
Size	Document Number		Rev
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**Main Func = Firmware SW**



## Firmware SW

Default setting:pull LOW  
DY for MP

05/15 SC

```

19  ME_FWP_SW>>>_____
24  ME_FWP    <<<_____

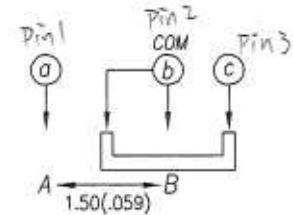
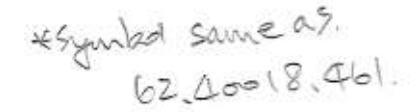
```

FSW1 change from 62.40018.691 to 62.40018.641  
20160623(DVT1)

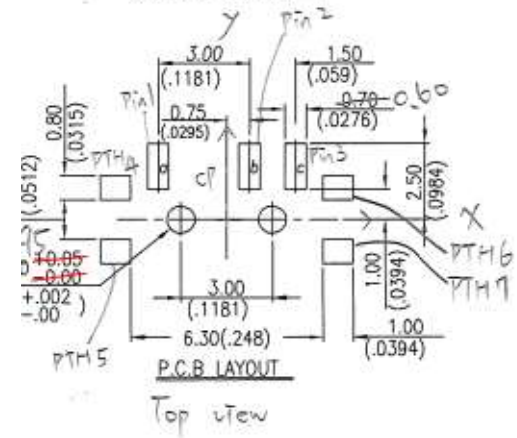
	3	1
	LOW	HIGH
ME_FWP	Normal Operation (Default)	Override

modify 20161122(X1)

modify 20161122(X1)



### CIRCUIT DIAGRAM



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## ***Firmware SW***

Size
A4

Document Number
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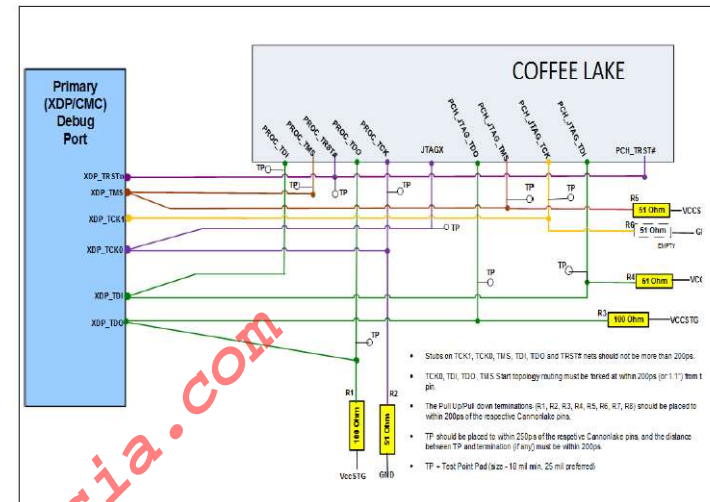
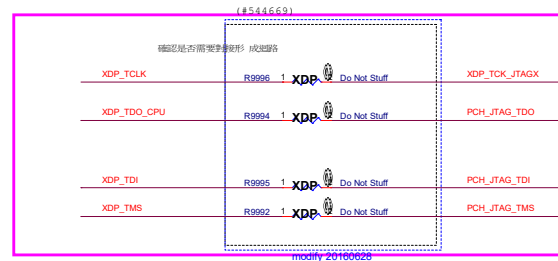
## Bucky WHL

Rev  
SA

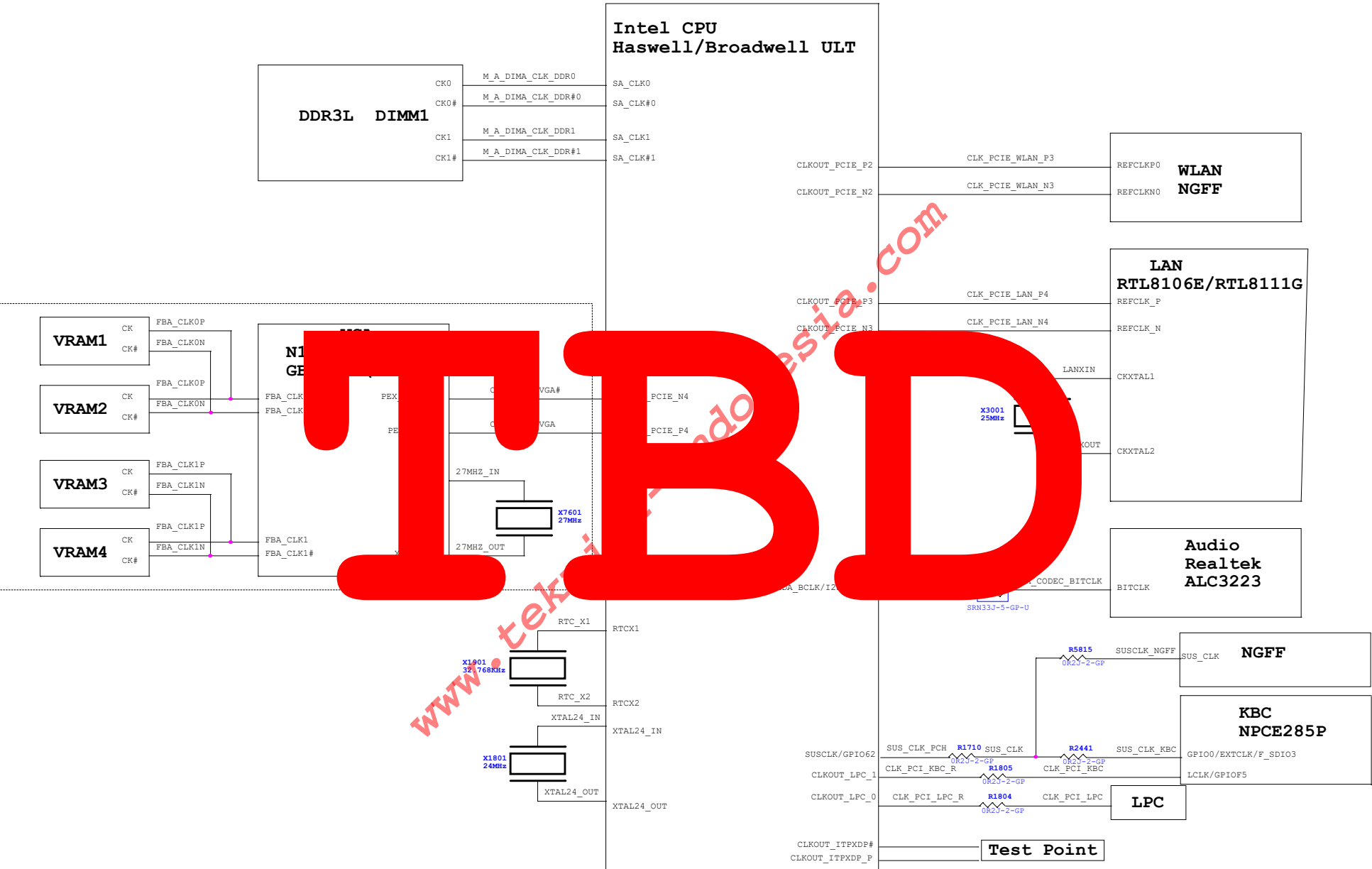
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3	XDP_TCLK	<<<—
3	XDP_TDO_CPU	<<<—
3	XDP_TDI	<<<—
3	XDP_TMS	<<<—
3	XDP_TCK_JTAGX	>>>—
3	PCH_JTAG_TDO	>>>—
3	PCH_JTAG_TDI	>>>—
3	PCH_JTAG_TMS	>>>—



CLK Block Diagram





[illegible]

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[illegible]

Timing diagram for RS to S0M0 [on Deep 3x Platform]. The diagram shows the timing relationships between various signals, including power rails, reset signals, and system status signals. Key signals include VccRTO, RTCRST#, VccDSW3\_3, DSW\_PWROK, BATLOW#, SLP\_SUS#, EXT\_PWR\_GATE#, PCH Pwm/Mphy Ralls, RSMRST#, SUSPWRODNACK, SUSCLK#, ACPRESENT, SUS\_ACK#, PWRBRTN#, SLP\_A#, Platform VccASW, SLP\_LAN#, Vcc\_LANPHY, SLP\_WLAN#, Vcc\_WLAN#, SLP\_S#, SLP\_S4#, SLP\_S3#, SLP\_S0#, ESPI\_RST#, CL\_RST#, VccST, VccPLL, VccSTG, VPP, VDDQ, VccPLL\_OC, VCCIO, VCCSA, VTT, DDR\_VTT\_CANTL, VDDQVWGOOD, IMVP\_VR\_READY, Platform S0 Ralls, ALL\_SYS\_PWRGD, VCCST\_PWRGD, PCH\_PWROK, PCH Clock Outputs, PROCPWRGOOD, IMVP\_VR\_ON, CPU SVID BUS, SYS\_PWROK, SUS\_STAT#, PLTRST#, VCC, VCCGT, THERMTRIP#, SPI Signals, and DDR\_RESE#.

The diagram includes several notes (Note 1 to Note 20) providing additional context and timing requirements. A large red watermark "Teknisi Indo" is overlaid on the diagram.

1V8\_AON

1V8\_MAIN

NVDD

NVDD05

PEX\_VDD

FINVD/Q

GC6

D3 Cold

GC6

D3 Cold

1V8\_MAIN must be powered down after NVDD is down.

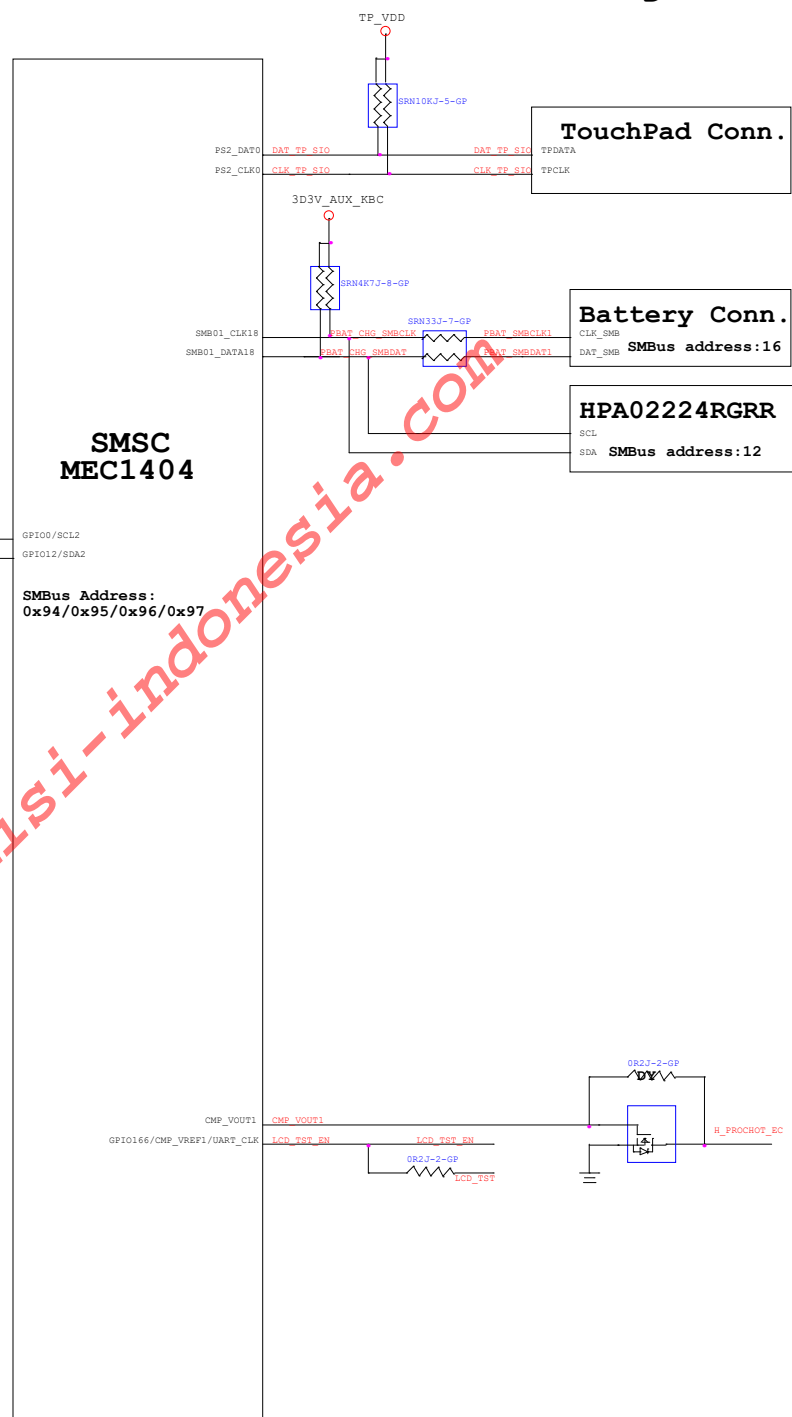
The diagram illustrates the power management architecture for the Skylake-U MCP. It shows the following components and their interconnections:

- Input Sources:** 3.3V, 5V, and 12V inputs are shown at the top left.
- Regulators:**
  - APL5930KAI:** A DC-DC converter that takes 10V<sub>IN</sub> and 10V<sub>OUT</sub> inputs.
  - SY8208DQBC:** A DC-DC converter that takes 10V<sub>IN</sub> and 10V<sub>OUT</sub> inputs.
  - M5938ARD1U:** A DC-DC converter that takes 10V<sub>IN</sub> and 10V<sub>OUT</sub> inputs.
  - G5016KD1U:** A DC-DC converter that takes 5V<sub>IN</sub> and 5V<sub>OUT</sub> inputs.
- Level Shifters:** Two level shifters are shown, one for the 10V<sub>OUT</sub> and one for the 5V<sub>OUT</sub>.
- Skylake-U MCP:** The central component, which is a multi-core processor. It has various power pins (e.g., 10V<sub>OUT</sub>, 5V<sub>OUT</sub>, 12V<sub>OUT</sub>) and is connected to the regulators and level shifters.
- KBC MEC1404:** A keyboard controller component connected to the Skylake-U MCP.

The diagram is annotated with a large red watermark 'mesia.com' and a large red 'X' over the top half. A legend at the bottom shows a sequence of numbers 1 through 10, each associated with a specific power rail or component.



### KBC SMBus Block Diagram



### Audio Block Diagram

